Masudul Hassan Quraishi

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Experience

- **Research Assistant** *Aug. 2019 - Present*
  Parallel Systems and Computing Laboratory (PSCLab) *Tempe, Arizona*
  - **Hardware Accelerators**: Research on FPGA architecture for OpenCL based hardware accelerator design and FPGA resource virtualization.
- **SoC Design Engineering Intern** *Jan. 2019 - August 2019*
  Intel Corporation *Santa Clara, California*
  - **RTL Design, Verification and Synthesis**: At Non-Volatile Memory Solutions Group (NSG), performed RTL Design and Basic Verification for the ECC Memory Blocks and optimized the architectures to reduce gate count and power consumption.
- **Research Assistant** *Aug. 2015 - Dec. 2018*
  Arizona Center for Integrative Modeling and Simulation (ACIMS) *Tempe, Arizona*
  - **Power Efficient Hardware Design and Prototyping**: Designed & tested power-optimized digital circuits using VHDL in Vivado Design Suite. Performed prototyping of the designs in FPGA using Xilinx Evaluation Kit.
- **Arizona State University** Tempe, Arizona
  Graduate Teaching Associate *Aug. 2015 - Present*
  - **Courses**: Principles of C++ Programming, Computer Organization and Assembly Language Programming, ASU MOOC-Introduction to Programming. Worked as an Instructor of Senior year Capstone Courses and Freshman year Introduction to Engineering Courses.
- **Joaquin Bustoz Math Science Honors Program (JBMSHP)** Tempe, Arizona
  Computer Lab Supervisor *Summer 2016 and 2017*
  - **MATLAB Tutorial**: Presented MATLAB Tutorials and Fundamental Statistics lectures to High School students attending Summer Math Science Program.

Education

- **Arizona State University** Tempe, Arizona
  PhD in Computer Engineering (Ongoing); *Aug. 2015 – December. 2022 (Expected)*
  - **Graduate Courses**: Hardware Acceleration and FPGA Computing, Computer Architecture II, Mobile Systems Architecture, Foundation of Algorithm, , Software Analysis and Design, Software Verification-Validation-Test
- **Bangladesh University of Engineering and Technology** Dhaka, Bangladesh
  Bachelor of Science in Electrical and Electronic Engineering; *Jan. 2008 – Feb. 2013*
  - **Undergraduate Courses**: Programming in C/C++, Numerical Analysis, Microprocessor and Interfacing

Projects

- **Hardware Accelerator**: Designed Hardware Accelerator for Bit-Q-Apriori algorithm in MATLAB and Simulink.
- **SRRIP Replacement Policy**: Implemented 2-bit SRRIP Block Replacement Policy using gem5 Simulator.
- **Speedy Tilt-Shift**: Designed and benchmarked Tilt-Shift functionality using Java, C++ and ARM NEON intrinsic in Android Studio. The implementations allows analyzing the performance implication of mobile image processing.
- **Podcast**: Developed Podcast, a news subscription system in Java using Publisher-Subscriber design pattern.

Publication

- **Masudul H. Quraishi**, Hessam Sarjoughian, Soroosh Gholami; *Co-simulation of Hardware RTL and Software System using FMI.* Proceedings of the 2018 Winter Simulation Conference, Gothenburg, Sweden. [PDF]

Technical Skills

- **Programming Languages**: OpenCL, C/C++, VHDL/Verilog/SystemVerilog, Java, MATLAB, MIPS Assembly, Python
- **IDE and Design Tools**: Vivado Design Suite, Intel Quartus, Modelsim, Simulink, Eclipse, LabVIEW, Microsoft Visual Studio, Simulink, Proteus, Cadence Virtuoso, Android Studio.
- **FPGA**: Working experience with Intel and Xilinx FPGAs