Dr. Fengbo Ren

Director, Parallel Systems and Computing Laboratory
Associate Professor, School of Computing and Augmented Intelligence
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RESEARCH INTERESTS

high-performance computing, reconfigurable computing, artificial intelligence, hardware-friendly deep learning, information-aware sensing, data-driven methods, IoT data analytics, edge computing, VLSI and embedded systems.

EDUCATION

University of California, Los Angeles, CA, USA (2010–2014)

Doctor of Philosophy in Electrical Engineering

Thesis: *A Scalable VLSI Architecture for Real-Time and Energy-Efficient Sparse Approximation in Compressive Sensing Systems*

Advisor: Dejan Marković | Parallel Data Architecture Group

Committee: Dejan Marković (Chair), Milos D. Ercegovac, Babak Daneshrad, William J. Kaiser

University of California, Los Angeles, CA, USA (2008-2010)

Master of Science in Electrical Engineering

Thesis: *Energy Performance Characterization of CMOS/Magnetic Tunnel Junction Hybrid Logic Circuits*

Advisor: Dejan Marković | Parallel Data Architecture Group

Committee: Dejan Marković (Chair), Kang L. Wang, Chih-Kong Ken Yang

Zhejiang University, Hangzhou, Zhejiang, China (2004–2008)

Bachelor of Engineering in Electrical Engineering

ACADEMIC EMPLOYMENT

Arizona State University, Tempe, AZ, USA, Jan. 2015 – now

Associate Professor, School of Computing and Augmented Intelligence, Aug. 2021 – now

Assistant Professor, School of Computing, Informatics and Decision Systems Engineering, Jan. 2015 – Aug. 2021

Graduate Faculty, School of Electrical, Computer and Energy Engineering

Honor Faculty, Barrett, the Honors College

Director, Parallel Systems and Computing Laboratory (PSCLab)

Other Affiliation: NSF I/UCRC Center for Embedded Systems (CES)

INDUSTRIAL EMPLOYMENT

Fellow Intern, Broadcom Inc., DSP Microelectronics, Irvine, CA, USA, Summer 2013

Involved in the low-power design of a 40nm 60GHz 802.11ad single-carrier decode system test-chip. Reduced the power consumption of key building blocks by 3x through architecture innovations.

Cisco Choice PhD Intern, Cisco Systems Inc., Data Center Group, San Jose, CA, Summer 2012

Led the FPGA emulation of a 480Gbps Data Center Switch ASIC (40nm).

Automated the hard-macro migration (SRAM, TCAM, TEMAC) from ASIC to FPGA.
Customized glue logic to integrate 1G PHY devices on board via GMII.
Successfully demoed the FPGA emulated network interface in a real Ethernet environment.

Digital ASIC Engineer Intern, QUALCOMM Inc., San Diego, CA, Fall 2009
Involved in the low power design of a 45nm smartphone SOC.
Investigated the clock gating and power gating efficiency.

RESEARCH ACTIVITIES AND EXPERIENCE

Principle Investigator, Arizona State University, Tempe, AZ, USA, 2015–Now

Active Research Programs

AP5. **A Data-Driven Approach for Scoring and Visualizing the Confidence of Segmentation**, **Single PI: Fengbo Ren**, ASU; Funding Source: TechInsights Inc., Period: Sep. 2021 – Aug. 2022, **Awarded Amount: $126,959.00** (Recognition: 100%).

AP4. **A Hybrid Approach for High-Accuracy Wiring/Via Segmentation**, **Single PI: Fengbo Ren**, ASU; Funding Source: TechInsights Inc., Period: Jan. 2021 – Dec. 2021, **Awarded Amount: $102,735.00** (Recognition: 100%).

AP3. **Compressive Learning for Energy-Efficient and Intelligent Internet-of-Things (IoT) — A System Framework from Data Compression to Decision Making (Year 2)**, **Single PI: Fengbo Ren**, ASU; Funding Source: Cisco Research Center, Award No.: CG#1490376, Period: Apr. 2020 – Sep. 2021, **Awarded Amount: $95,000.00** (Recognition: 100%).

AP2. **CAREER: Building Energy-Efficient IoT Frameworks - A Data-Driven and Hardware-Friendly Approach Tailored for Wearable Applications**, **Single PI: Fengbo Ren**, ASU; Funding Source: National Science Foundation (NSF), Award No.: 1652038, Period: Feb. 2017 – Jan. 2022, **Awarded Amount: $534,225.00 + $16,000.00 REU Supplement** (Recognition: 100%).

AP1. **II-NEW: GEARS - An Infrastructure for Energy-Efficient Big Data Research on Heterogeneous and Dynamic Data**, PI: M. Zhao, ASU, **Co-PI: Fengbo Ren**, H. Liu, K. S. Candan, H. Davulcu, ASU; Funding Source: National Science Foundation (NSF), Award No.: 1629888, Period: Sep. 2016 – Aug. 2021, **Awarded Amount: $750,000.00** (Recognition: 16%).

Completed Research Programs

CP7. **Visual Analytics on Edge**, **Single PI: Fengbo Ren**, ASU; Funding Source: RadiusAI Inc., Period: Mar. 2019 – Mar. 2020, **Awarded Amount: $20,000.00** (Recognition: 100%).

CP6. **Hardware-based Machine Learning**, **PI:** Asim Roy, ASU, **Co-PI: Fengbo Ren**, ASU; Funding Source: Aviage Systems, Period: Jan. 2018 – Dec. 2018, **Awarded Amount: $30,000.00** (Recognition: 67%).

CP5. **Towards Energy-Efficient and Intelligent Internet-of-Things (IoT) — A System Framework from Data Compression to Decision Making (Year 1)**, **Single PI: Fengbo Ren**, ASU; Funding Source: Cisco Research Center, Award No.: CG#1319167, Period: Aug 2018 – Sep. 2019, **Awarded Amount: $126,926.00** (Recognition: 100%).

CP4. **Neural Network Based Video Compression: A Real-time End-to-end Learning Framework for High-Frame-Rate Camera, Single PI: Fengbo Ren,** ASU; Funding Source: Google Research, Google LLC, Period: Mar. 2018 – Mar. 2019, **Awarded Amount: $51,417.00** (Recognition: 100%).

CP3. **Building Energy-Efficient Data Center Accelerator for Deep Neuron Network by Harnessing the Power of Multi-FPGA Cluster**, **Single PI: Fengbo Ren**, ASU; Funding Source: Cisco Research Center, Award No.: CG#594589, Period: May 2016 – Dec. 2017, **Awarded Amount: $99,992.00** (Recognition: 100%).

CP2. **Building Data-Driven Compressive Sensing Based Wireless Sensor Node for Personalized IoT**, **PI: Fengbo Ren**, ASU (Administrative co-PI is the CES director, Dr. Vrudhula); Funding Source: Center for Embedded System (CES) at ASU, Award No.: A4.Y8.FR, Period: Sep. 2016 – Aug. 2017, **Awarded Amount: $32,000.00** (Recognition: 0%).

CP1. **Building Energy-Efficient, Adaptive, and Secure Wireless Sensor Node**, **PI: Fengbo Ren**, ASU (Administrative co-PI is the CES director, Dr. Vrudhula); Funding Source: Center for Embedded System (CES) at ASU, Award No.: A4.Y7.FR, Period: Sep. 2015 – Aug. 2016, **Awarded Amount: $47,500.00** (Recognition: 0%).

Research Assistant, Parallel Data Architecture Group, University of California, Los Angeles, CA, USA, 2009–2014

- **Energy-Delay Characterization of Magnetic Tunnel Junction based Circuits**
  Results published in IEEE Transactions on Electron Devices—the top journal in the IEEE Electron Device Society.
- **Spin-torque-transfer Random Access Memory (STT-RAM) Design**
  Involved in two successful tape-out in IBM 65nm and 45nm SOI CMOS technology as one of the main designers. The research outcome has resulted in 1 international patent.
- **VLSI Architecture for Compressive Sensing and Sparse Signal Processing**
  Results published in International Solid-State Circuits Conference (ISSCC) and in IEEE Journal of Solid-State Circuits (as an invited paper)—the top conference and top journal in the IEEE Solid-State Circuits Society, respectively. The research outcome has resulted in 1 U.S. patent.

PUBLICATIONS

[Publication Archive Page] [Google Scholar Page]

Legend: (*) Corresponding Author; **Bold Font**: ASU Ph.D. Student for whom Dr. Ren is the primary advisor; ***Bold Italic Font***: ASU Ph.D. Student for whom Dr. Ren is a co-advisor or has significant mentoring responsibility; Underline Font: ASU Master Student for whom Dr. Ren is the primary advisor or a co-advisor; (#) ASU Undergraduate Student; (∞) Other/Visiting Student; (✕) ASU Postdoctoral Researcher; (‡) High School Student; (+) Equal Contributions; (~) Presenting Author.

Manuscripts

M7. **Zifan Yu***, Suya You, Fengbo Ren, “Frequency-domain Learning for Volumetric-based 3D Data Perception”, manuscript in preparation.

M6. **Erfan Bank Tavakoli***, **Masudul Quraishi+**, **Michael Riera+**, and Fengbo Ren, “FSpGEMM: An OpenCL-based HPC Framework for Accelerating General Sparse Matrix-Matrix Multiplication on FPGAs”, under review.

M5. **Erfan Bank Tavakoli***, **Masudul Quraishi+**, **Michael Riera+**, and Fengbo Ren, “FSCHOL: An OpenCL-based HPC Framework for Accelerating Sparse Cholesky Factorization on FPGAs”, under review.

M4. **Michael Riera*, Masudul Quraishi+, Erfan Bank Tavakoli+**, and Fengbo Ren, “FLASH 1.0: A Software Framework for Rapid Parallel Deployment and Enhancing Host Code Portability in Heterogeneous Computing”, under review.

M3. **Michael Riera*, Masudul Quraishi+, Erfan Bank Tavakoli+**, and Fengbo Ren, “HALO 1.0: A Hardware-agnostic Accelerator Orchestration Framework for Enabling Hardware-agnostic Programming with True Performance Portability for Heterogeneous HPC”, under review.

M2. **Zhikang Zhang*~, Kai Xu,** and Fengbo Ren, "Selective Sensing: A Data-driven Nonuniform Subsampling Approach for On-sensor Data Dimensionality Reduction", under review.

M1. Akshay Dua*~, **Yixing Li**, and Fengbo Ren, "Systolic-CNN: An OpenCL-defined Scalable Run-time-flexible FPGA Accelerator Architecture for Accelerating Convolutional Neural Network Inference in Cloud/Edge Computing", *under review.*

Master Theses

Th3. Akshay Dua, "A Scalable Parameterized OpenCL-Defined Accelerator Architecture for Efficient Convolutional Neural Network (CNN) Inference on FPGAs", *Master Thesis,* School of Computing, Informatics, and Decision Systems Engineering, Arizona State University, Dec. 2019.

Th2. Aswin Gunavelu Mohan, "Hardware Acceleration of Most Apparent Distortion Image Quality Assessment Algorithm on FPGA Using OpenCL", *Master Thesis,* School of Computing, Informatics, and Decision Systems Engineering, Arizona State University, May 2017.

Th1. Fengbo Ren, "Energy-performance Characterization of CMOS/Magnetic Tunnel Junction (MTJ) Hybrid Logic Circuits", *Master Thesis,* Department of Electrical Engineering, University of California, Los Angeles, Dec. 2011.

Ph.D. Dissertations

D3. **Kai Xu**, "Learning in Compressed Domains", *Ph.D. Dissertation,* School of Computing, Informatics, and Decision Systems Engineering, Arizona State University, May 2021.

D2. **Yixing Li**, "Hardware-Friendly Deep Learning for Edge Computing", *Ph.D. Dissertation,* School of Computing, Informatics, and Decision Systems Engineering, Arizona State University, May 2021.

D1. Fengbo Ren, "A Scalable VLSI Architecture for Real-Time and Energy-Efficient Sparse Approximation in Compressive Sensing Systems", *Ph.D. Dissertation,* Department of Electrical Engineering, University of California, Los Angeles, Jan. 2015.

Peer-Reviewed Journal Articles

J18. Jonathan Zhao∞*, Márk Lakatos-Tóth∞, Matthew Westerham∞, **Zhikang Zhang**, Avi Moskoff∞, Fengbo Ren, "OpenICS: Open Image Compressive Sensing Toolbox and Benchmark", *Software Impacts,* vol. 9, Aug. 2021.

J17. **Masudul Quraishi*+, Erfan Bank Tavakoli+,** and Fengbo Ren, "A Survey of System Architectures and Techniques for FPGA Virtualization", *IEEE Transactions on Parallel and Distributed Systems (**TPDS**),* vol. 32, no. 9, pp. 2216-2230, 2021.

J16. **Yixing Li***, Shuai Zhang, Xichuan Zhou, and Fengbo Ren, "Build a Compact Binary Neural Network through Bit-level Sensitivity and Data Pruning", ***Neurocomputing**,* vol. 398, pp. 45-54, Jul. 2020.

J15. Ying Wei*, Jun Zhou, Yin Wang, Yinggang Liu, Qingsong Liu, Jiansheng Luo, Chao Wang, Fengbo Ren, Li Huang, "A Review of Algorithm & Hardware Design for AI-Based Biomedical Applications", *IEEE Transactions on Biomedical Circuits and Systems (**TBioCAS**),* vol. 14, no. 2, pp. 145-163, 2020.

J14. Yujie Feng*, Fan Yang, Xichuan Zhou, Yanli Guo, Fang Tang, Fengbo Ren, Jishun Guo, Shuiwang Ji, "A Deep Learning Approach for Targeted Contrast-Enhanced Ultrasound Based Prostate Cancer Detection", *IEEE/ACM Transactions on Computational Biology and Bioinformatics (**TCBB**),* vol. 16, no. 6, pp. 1794-1801, 2019.

J13. **Yixing Li*,** Zichuan Liu, Wenye Liu, Yu Jiang, Yongliang Wang, Wang Ling Goh, Hao Yu, Fengbo Ren, "A 34-FPS 698-GOP/s/W Binarized Deep Neural Network-Based Natural Scene Text Interpretation Accelerator for Mobile Edge Computing", *IEEE Transactions on Industrial Electronics (**TIE**),* vol. 66, no. 9, pp. 7407-7416, Sep. 2019.

J12. **Yixing Li***, Zichuan Liu, **Kai Xu,** Hao Yu, and Fengbo Ren, "A GPU-Outperforming FPGA Accelerator Architecture for Binary Convolutional Neural Networks", *ACM Journal on Emerging Technologies in Computing Systems (**JETC**)—Special Issue on Frontiers of Hardware and Algorithms for On-chip Learning,* vol. 14, no. 2, p. 18, 2018.

J11. Yuhao Wang*∞, Xin Li, **Kai Xu**, Fengbo Ren, Hao Yu, "Data-Driven Sampling Matrix Boolean Optimization for Energy-Efficient Biomedical Signal Acquisition by Compressive Sensing", *IEEE Transactions on Biomedical Circuits and Systems (**TBioCAS**)*, vol. 11, no. 2, pp. 255-266, Nov. 2016.

J10. Boyu Hu*, Fengbo Ren, Zuow-Zun Chen, Xicheng Jiang, Mau-Chung Frank Chang, "An 8-Bit Compressive Sensing ADC with 4-GS/s Equivalent Speed Utilizing Self-Timed Pipeline SAR-Binary-Search", *IEEE Transactions on Circuits and Systems II: Express Briefs (**TCAS-II**),* vol. 63, no. 10, pp. 934-938, Oct. 2016.

J9. Boyu Hu*, Fengbo Ren, Zuow-Zun Chen, Xicheng Jiang, Mau-Chung Frank Chang, "9-bit time–digital-converter-assisted compressive-sensing analogue–digital-converter with 4 GS/s equivalent speed", *IET Electronics Letters (**EL**),* vol. 52, no. 6, pp. 430-432, Mar. 2016.

J8. **(Invited)** Fengbo Ren* and Dejan Marković, "A Configurable 12-to-237KS/s 12.8mW Sparse-Approximation Engine for Mobile Data Aggregation of Compressively Sampled Physiological Signals", *IEEE Journal of Solid-State Circuits **(JSSC)**,* vol. 51, no. 1, pp. 68-78, Jan. 2016.

J7. Junpeng Li*, Jiajie Liang, Lu Li, Fengbo Ren, Wei Hu, Juan Li, Shuhua Qi, Qibing Pei, "Healable Capacitive Touch Screen Sensors Based on Transparent Composite Electrodes Comprising Silver Nanowires and a Furan/Maleimide Diels–Alder Cycloaddition Polymer", ***ACS Nano**,* vol. 8, no. 12, pp. 12874-12882, Dec. 2014.

J6. Fengbo Ren*, Chenxin Zhang, Liang Liu, Wenyao Xu, Victor Öwall, and Dejan Marković, "A Square-Root-Free Matrix Decomposition Method for Energy-Efficient Least Square Computation on Embedded Systems", *IEEE Embedded Systems Letters (**ES**),* vol. 6, no. 4, pp. 73-76, Dec. 2014.

J5. Lerong Cheng*, Wenyao Xu, Fengbo Ren, Fang Gong, Puneet Gupta, and Lei He, "Statistical Timing and Power Analysis of VLSI Considering Non-Linear Dependence", *Integration, the VLSI Journal (**INTEG**),* vol. 47, no. 4, pp. 487-498, Sep. 2014.

J4. Fengbo Ren*, Wenyao Xu, and Dejan Marković, "Scalable and Parameterized VLSI Architecture for Efficient Sparse Approximation in FPGAs and SoCs", *IET Electronics Letters (**EL**),* vol. 49, no. 23, pp. 1440-1441, Nov. 2013.

J3. Fengbo Ren*, Henry Park, Chih-Kong Ken Yang, and Dejan Marković, "Reference Calibration of Body-Voltage Sensing Circuit for High-Speed STT-RAMs", *IEEE Transactions on Circuits And Systems—I: Regular Papers (**TCAS-I**),* vol. 60, no. 11, pp. 2932-2939, Nov. 2013.

J2. Richard Dorrance*, Fengbo Ren, Yuta Toriyama, Amr Amin Hafez, Chih-Kong Ken Yang, and Dejan Marković, "Scalability and Design-Space Analysis of a 1T-1MTJ Memory Cell for STT-RAMs," *IEEE Transactions on Electron Devices (**TED**),* vol. 59, no. 4, pp. 878-887, Apr. 2012.

J1. Fengbo Ren*, and Dejan Marković, "True Energy-Performance Analysis of the MTJ-Based Logic-in-Memory Architecture (1-Bit Full Adder)," *IEEE Transactions on Electron Devices (**TED**),* vol. 57, no. 5, pp. 1023-1028, May 2010.

Peer-Reviewed Conference and Workshop Papers

C22. Xichuan Zhou*, Yicong Peng, Chunqiao Long, Fengbo Ren, Cong Shi, "MoNet3D: Towards Accurate Monocular 3D Object Localization in Real Time", *The Thirty-seventh International Conference on Machine Learning (**ICML'20**),* Virtual Event, Jul. 2020, PMLR 119:11503-11512.

C21. **Kai Xu*~,** Minghai Qin, Yuhao Wang, Y.-K. Chen, and Fengbo Ren, "Learning in the Frequency Domain", *The Conference on Computer Vision and Pattern Recognition (**CVPR'20**),* Seattle,

Washington, Jun. 2020, pp. 1740-1749.

C20. **Zhikang Zhang*~, Kai Xu,** and Fengbo Ren, "CRA: A Generic Compression Ratio Adapter for End-to-end Data-driven Compressive Sensing Reconstruction Frameworks", *the 45th International Conference on Acoustics, Speech, and Signal Processing (**ICASSP'20**),* May 2020, pp. 1439-1443.

C19. **Yixing Li*~,** Akshay Dua, and Fengbo Ren, "Light-Weight RetinaNet for Object Detection on Edge Devices", *The 2020 IEEE World Forum on Internet of Things (**WF-IoT'20**),* New Orleans, Louisiana, Apr. 2020, to appear.

C18. **(Invited) Yixing Li*~,** and Fengbo Ren, "BNN Pruning: Pruning Binary Neural Network Guided by Weight Flipping Frequency", *21st International Symposium on Quality Electronic Design (**ISQED'20**),* Mar. 2020.

C17. **Kai Xu*~**, **Zhikang Zhang**, and Fengbo Ren, "LAPRAN: A Scalable Laplacian Pyramid Reconstructive Adversarial Network for Flexible Compressive Sensing Reconstruction", *the 15th European Conference on Computer Vision (**ECCV'18**),* Sep. 2018, pp. 491-507.

C16. **Saman Biookaghazadeh*~**, Ming Zhao, and Fengbo Ren, "Are FPGAs Suitable for Edge Computing?", *The USENIX Workshop on Hot Topics in Edge Computing (**HotEdge '18**),* June 2018.

C15. Zichuan Liu*~, **Yixing Li,** Fengbo Ren, Hao Yu, and Wang Ling Goh, "SqueezedText: A Real-time Scene Text Recognition by Binary Convolutional Encoder-decoder Network", *the AAAI Conference on Artificial Intelligence (**AAAI'18**),* Apr. 2018, pp. 7194-7201.

C14. **Kai Xu*~**, and Fengbo Ren**,** "CSVideoNet: A Real-time End-to-end Learning Framework for High-frame-rate Video Compressive Sensing", *IEEE Winter Conf. on Applications of Computer Vision (**WACV'18**),* Mar. 2018, pp. 1680-1688.

C13. **Kai Xu*~**, **Yixing Li**, and Fengbo Ren, "A Data-Driven Compressive Sensing Framework Tailored For Energy-Efficient Wearable Sensing", in *Proceedings of the 42nd IEEE International Conference on Acoustics, Speech and Signal Processing (**ICASSP'17**)*, Mar. 2017, pp. 861-865.

C12. Zichuan Liu*~, **Yixing Li**, Fengbo Ren, and Hao Yu, "A Binary Convolutional Encoder-decoder Network for Real-time Natural Scene Text Processing", *the 1st International Workshop on Efficient Methods for Deep Neural Networks in the Conference on Neural Information Processing Systems (**NIPS'16**),* Dec. 2016.

C11. H. Huang*~, Hao Yu, Cheng Zhou, and Fengbo Ren, "A Compressive-sensing based Testing Vehicle for 3D TSV Pre-bond and Post-bond Testing Data", in *Proceedings of the International Symposium on Physical Design (**ISPD'16**)*, Apr. 2016, pp. 19-25.

C10. **Kai Xu*~**, **Yixing Li**, and Fengbo Ren, "An Energy-Efficient Compressive Sensing Framework Incorporating Online Dictionary Learning for Long-Term Wireless Health Monitoring", in *Proceedings of the 41st IEEE International Conference on Acoustics, Speech and Signal Processing (**ICASSP'16**), Mar. 2016, pp. 804-808.*

C9. Fengbo Ren*~, and Dejan Marković, "A Configurable 12-to-237KS/s 12.8mW Sparse-Approximation Engine for Mobile ExG Data Aggregation", in *Proceedings of IEEE International Solid-State Circuits Conference (**ISSCC'15**),* Feb. 2015, pp. 334-335.

C8. Richard Dorrance*~, Fengbo Ren, and Dejan Marković, "An Efficient Sparse Matrix-Vector Multiplication (SpMxV) Kernel For Sparse-BLAS on FPGAs", in *Proceedings of 21st ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (**FPGA'14**),* Feb. 2014, pp. 161-170.

C7. Xiaoyi Zhang*~, Ming-Chun Huang*, Fengbo Ren*, Wenyao Xu*, Nan Guan*, and Wang Yi*, "Proper Running Posture Guide: A Wearable Biomechanics Capture System", in *Proceedings of 8th International Conference on Body Area Networks (**BodyNets'13**), Oct. 2013,* pp. 83-89.

C6. Xiaoyi Zhang*~, Wenyao Xu, Ming-Chun Huang, Navid Amini, and Fengbo Ren, "See UV on Your Skin:

An Ultraviolet Sensing and Visualization System", in *Proceedings of the 8th International Conference on Body Area Networks (**BodyNets'13**), Oct. 2013*, pp. 22-28.

C5. Fengbo Ren*, Richard Dorrance**~**, Wenyao Xu and Dejan Marković, "A Single-Precision Compressive Sensing Signal Reconstruction Engine on FPGAs", in *Proceedings of 23rd International Conference on Field Programmable Logic and Applications (**FPL'13**),* Sep. 2013, pp. 1-4.

C4. Wenyao Xu*~, Ming-Chun Huang, Jason J. Liu, Fengbo Ren, Xinchen Shen, Xiao Liu, and Majid Sarrafzadeh, "Mobile Phone Based Lung Function Diagnosis and Exercise System for COPD", *Proceedings of International Conference on Pervasive Technologies Related to Assistive Environments (**PETRA'13**),* May 2013, pp. 45-52.

C3. Fengbo Ren*~, Henry Park, Richard Dorrance, Yuta Toriyama, Chih-Kong Ken Yang, and Dejan Marković, "A Body-Voltage-Sensing-Based Short Pulse Reading Circuit for Spin-Torque Transfer RAMs (STT-RAMs)," in *Proceedings of 13th International Symposium on Quality Electronic Design (**ISQED'12**),* Mar. 2012, pp. 275-282.

C2. Henry Park*~, Richard Dorrance, Amr Amin Hafez, Fengbo Ren, Dejan Marković, and Chih-Kong Ken Yang, "Analysis of STT-RAM Cell Design with Multiple MTJs Per Access," in *Proceedings of ACM/IEEE International Symposium on Nanoscale Architectures (**NANOARCH'11**),* Jun. 2011, pp. 32-36.

C1. Richard Dorrance*~, Fengbo Ren, Yuta Toriyama, Amr Amin Hafez, Chih-Kong Ken Yang, and Dejan Marković, "Scalability and Design-Space Analysis of a 1T-1MTJ Memory Cell," in *Proceedings of ACM/IEEE International Symposium on Nanoscale Architectures (**NANOARCH'11**),* Jun. 2011, pp. 53-58.

Peer-Reviewed Conference Abstracts

A2. Akshay Dua*~, **Yixing Li**, and Fengbo Ren, "Systolic-CNN: An OpenCL-defined Scalable Run-time-flexible FPGA Accelerator Architecture for Accelerating Convolutional Neural Network Inference in Cloud/Edge Computing", *The 28th The International Conference on Field-Programmable Logic and Applications (**FPL'20**)*, under review.

A1. **Yixing Li*~**, Zichuan Liu, **Kai Xu,** Hao Yu, and Fengbo Ren, "A 7.663-TOPS 8.2-W Energy-efficient FPGA Accelerator for Binary Convolutional Neural Networks", in *Proceedings of the 2017 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (**FPGA'17**),* Feb. 2017, pp. 290-291.

Patents

P12. **Zhikang Zhang,** and Fengbo Ren, "Selective Sensing: A Data-Driven Nonuniform Subsampling Approach For Computation-Free On-Sensor Data Dimensionality Reduction", *U.S. Patent Pending,* 63/022,735, May 2021.

P11. **Yixing Li**, and Fengbo Ren, "Systems and Methods for Pruning Binary Neural Networks Guided By Weight Flipping Frequency", *U.S. Patent Pending,* 63/022,913, May 2021.

P10. Akshay Dua, and Fengbo Ren, "Systolic-CNN: An OpenCL-defined Scalable Run-time-flexible FPGA Accelerator Architecture or Efficient Convolutional Neural Network (CNN) Inference in Cloud/Edge Computing", *U.S. Patent Pending,* 63/016,434, Apr. 2021.

P9. **M. Riera**, Fengbo Ren, **M. H. Quraishi**, and **E. Bank-Tavakoli**, "A Software-Defined Board Support Package (SW-BSP) for Stand-Alone Reconfigurable Accelerators", *International Patent Pending,* PCT/US2021/020355*,* Mar. 2020.

P8. **M. Riera**, Fengbo Ren, **M. H. Quraishi**, and **E. Bank-Tavakoli**, "A Stand-Alone Accelerator Protocol (SAP) for Heterogeneous Computing Systems", *International Patent Pending,* PCT/US2021/020354*,* Mar. 2020.

P7. **M. Riera**, Fengbo Ren, **M. H. Quraishi**, and **E. Bank-Tavakoli**, "HALO: A Hardware-Agnostic Accelerator Orchestration Software Framework for Heterogeneous Computing Systems", *International Patent Pending,* PCT/US2021/020352*,* Mar. 2020.

P6. **M. Riera**, Fengbo Ren, **M. H. Quraishi**, and **E. Bank-Tavakoli**, "C2MPI: A Hardware-Agnostic Message Passing Interface for Heterogeneous Computing Systems", *International Patent Pending,* PCT/US2021/020353*,* Mar. 2020.

P5. **Zhikang Zhang**, Fengbo Ren, and **Kai Xu**, "Generic Compression Ratio Adapter for End-to-end Data-driven Compressive Sensing Reconstruction Frameworks", *U.S. Patent Pending,* 63/002,770, Mar. 2021.

P4. Fengbo Ren, and **Kai Xu**, "LAPRAN: A Scalable Laplacian Pyramid Reconstructive Adversial Network for Flexible Compressive Sensing Reconstruction", *US Patent Pending*, US20200234406, Jul. 2020.

P3. Fengbo Ren, and **Kai Xu**, "CSVideoNet: A Real-time End-to-end Learning Framework for High-frame-rate Video Compressive Sensing", *U.S. Patent,* US20190124346, Apr. 2019.

P2. Dejan Marković, and Fengbo Ren, "A Scalable and Parameterized VLSI Architecture for Compressive Sensing Sparse Approximation", *U.S. Patent,* US20150032990 A1, Jan. 2015.

P1. K.-L. Wang, C.-K. Yang, Dejan Marković, and Fengbo Ren, "Body Voltage Sensing Based Short Pulse Reading Circuit", *International Patent*, WO2013043738 A1, Mar. 2013.

TALKS AND PRESENTATIONS

Conference Tutorials

Tu1. Baoxin Li, and Fengbo Ren, "Machine & Deep Learning for Edge-Cloud Computing Systems", International Symposium on Circuits and Systems (ISCAS'19), Sapporo, Japan, May 26th, 2019.

Invited Talks in Research Seminars and Colloquia

T17. "Compressive Sensing in Wireless Health Monitoring: From Theory to Hardware Implementations", *Research Seminar,* Hiroshima University, Japan, Aug. 4th, 2017.

T16. "Compressive Sensing in Wireless Health Monitoring: From Theory to Hardware Implementations", *Research Seminar,* Zhejiang University, China, Jul. 29th, 2016.

T15. "Compressive Sensing in Wireless Health Monitoring: From Theory to Hardware Implementations", *Research Seminar,* Zhejiang University, China, Jul. 29th, 2016.

T14. "Compressive Sensing in Wireless Health Monitoring: From Theory to Hardware Implementations", *Research Seminar,* Chongqing University, China, Jul. 27th, 2016.

T13. "Compressive Sensing in Wireless Health Monitoring: From Theory to Hardware Implementations", *Research Seminar,* Beijing Microelectronics Technology Institute, China Jul. 25th, 2016.

T12. "VLSI Design to the Rescue: Building Future Application Drivers with Energy Efficiency", *EECS Research Seminar,* Case Western Reserve University, Mar. 3rd, 2015.

T11. "VLSI Design to the Rescue: Building Future Application Drivers with Energy Efficiency", *Electrical & Computer Engineering Research Seminar,* Wayne State University, Apr. 9th, 2014.

T10. "VLSI Design to the Rescue: Building Future Application Drivers with Energy Efficiency", *EECS Research Seminar Series,* University of Kansas, Apr. 7th, 2014.

T9. "VLSI Design to the Rescue: Building Future Application Drivers with Energy Efficiency", *Computer Science & Engineering Colloquia Series,* Washington University in St. Louis, Apr. 3rd, 2014.

T8. "VLSI Design to the Rescue: Building Future Application Drivers with Energy Efficiency*", Iowa Informatics Initiative Research Seminar,* University of Iowa, Mar. 26th, 2014.

T7. "VLSI Design to the Rescue: Building Future Application Drivers with Energy Efficiency", *Electrical Engineering Seminar,* Southern Methodist University, Mar. 18th, 2014.

T6. "VLSI Design to the Rescue: Building Future Application Drivers with Energy Efficiency", *Research Seminar Series,* Arizona State University, Mar. 4th, 2014.

T5. "VLSI Design to the Rescue: Building Future Application Drivers with Energy Efficiency, *Electrical and Computer Engineering Colloquia,* University of Rochester, Feb. 26th, 2014.

T4. "VLSI Design for Compressive Sensing Signal Reconstruction", *Faculty Lunch Forum,* University of California, Los Angeles, Nov. 20th, 2013.

T3. "VLSI Design for Compressive Sensing (CS) Applications", *Broadcom Integrated Circuits Fellowship Program Workshop,* University of California, Los Angeles, Oct. 14th, 2013.

T2. "Sparse Signal Decoder for Compressive Sensing (CS) Applications", *Annual Research Review,* University of California, Los Angeles, Dec. 17th, 2012.

T1. "Energy-Performance Characterization of CMOS/MTJ Hybrid-Logic Architectures", *NRI Architecture & Device Benchmarking Workshop,* University of Notre Dame, Aug. 11th, 2010.

Invited Talks and Outreach to Industry or Research Sponsors

T11. "A Hybrid Approach for High-Accuracy Wiring/Via Segmentation", TechInsights/ASU Project Proposal Meeting, May 12th, 2020.

T10. "Chip Design and Pattern Recognition", TechInsights ASU Visit Meeting, January 8th, 2020.

T9. "Hardware Acceleration for Video Analytics on FPGA using OpenCL", RadiusAI Research Project Meeting, Sep. 24th, 2020.

T8. "OpenCL-based FPGA Acceleration Framework for Object Detection", RadiusAI Research Project Meeting, Apr. 5th, 2019.

T7. "ECDI: A Virtual Heterogeneous Edge Server Platform (vHESP) for Data-flow-centric, Multi-tenancy, and Secure Edge Computing", *NSF/VMware Partnership on Edge Computing Data Infrastructure (ECDI) Reverse Site Review,* July 13th, 2018.

T6. "Performance Characterization of OpenCL Kernels on Heterogeneous Computing Platforms", Cisco Research Project Meeting, Sep. 7th, 2017.

T5. "Deep FPGA Accelerator for Binary Convolution Neural Network", Cisco Research Project Meeting, Sep. 7th, 2017.

T4. "FPGA Acceleration for Binary Convolutional Neural Networks", Cisco Research Project Meeting, Nov. 11th, 2016.

T3. "Compressive Sensing (CS): Theory, Applications, and VLSI Design", *Broadcom DSP Microelectronics Chalk Talk,* Broadcom Inc., Irvine, California, Jul. 3rd, 2013.

T2. "Sparse Signal Decoder for Compressive Sensing (CS) Applications", *Broadcom Fellowship Meeting,* Broadcom Inc., Irvine, California, Apr. 26th, 2013.

T1. "Spin-Transfer Torque Random Access Memory (STT-RAM)", *Cisco Training Session (Webex),* Dec. 4th, 2011.

ASU Seminars, Workshops and Guest Lectures

T4. "Empowering Edge Computing with FPGAs", *Planning Workshop of Industry University Cooperative Research Center for Network-Embedded, Smart and Safe Things (NESST),* May 16th, 2019.

T3. "Hardware Acceleration and FPGA Computing", Guest Lecture in CSE 420 Computer Architecture I, Jun. 21st, 2017.

T2. "Compressive Sensing: From Theory to Hardware Implementation", *Spring 2016 Faculty Talk Series,* School of Computing, Informatics, and Decision Systems Engineering, Arizona State University, Mar. 26th, 2016.

T1. "A Configurable Sparse-Approximation Engine for Mobile Data Aggregation of Compressively Sampled Physiological Signals", *Workshop: Flexible Reconfigurable Electronics: 2D Devices and*

Materials, Arizona State University, Apr. 24th, 2015.

TEACHING EXPERIENCE

Legend: (#) New Course Developed; (‡) Course Redesigned.

Faculty, Computer Science and Engineering, Arizona State University, Tempe, AZ, USA

- **(Spring 2021) CSE 320: Design/Synthesis of Digital Hardware‡** | *Teaching Eval: 4.37 / 5.0*
  Enrollment Size: 40; Some student comments: *"The lectures and pacing of course content is amazing." | "The professor is what I like the most about this course. He gives tips on what can be applied to interviews, on how theory can be applied to a real-world application, it's good stuff. He also comes across as genuine and wants to help us succeed."*
- **(Spring 2021) CEN 571: Hardware Acceleration and FPGA Computing#** | *Teaching Eval: 4.19 / 5.0*
  Enrollment Size: 22; Some student comments: *"Even though this course is an iCourse, the videos were evident and had all the details needed for the assignment and homework. I really liked the way the professor has explained the concepts. Almost all the questions that arose in my mind were clearly explained in the video. The course work is well planned, and the flow didn't break for the entire semester. This is one of the best courses that I have taken this semester."*
- **(Fall 2020) CEN 571: Hardware Acceleration and FPGA Computing#** | *Teaching Eval: 4.67 / 5.0*
  Enrollment Size: 123; Some student comments: *"The course is well structured and touches on all the important nuances in this field." | "The lectures and notes cover many important aspects of HW accelerators and optimization techniques in great detail." | "Though remote, class was handled very well, and Professor was very considerate regarding deadlines. Thanks for a wonderful class!" | "The course gives a thorough understanding of FPGA and ASIC design from a hardware-software co-optimization angle. This course gave a new insight into how to look at the design and algorithms." | "I would like to take a moment and appreciate the professor and everyone who designed the course because it explains a lot of concepts in the ASIC and FPGA design and the Homework is designed to support the concepts and I would like to say that I love this course would recommend this course any day." | "Professor's approach and clarity of explanation made me enthusiastic to listen to his lectures."*
- **(Spring 2020) CSE 320: Design/Synthesis of Digital Hardware‡** | *Teaching Eval: 4.42 / 5.0*
  Enrollment Size: 60; Some student comments: *"Fengbo is obviously a smart and passionate teacher with a great deal of expertise in the field." | "I like that the professor related what we were learning to real world examples." | "Professor Ren Is one of the best professors I've taken here and I only wish I had more classes with him." | "Professor Ren cared about the students and he was super helpful to save a student from not understanding anything about the course's concepts." | "Dr. Ren is an absolutely fantastic lecturer, you can tell he has great passion in his line of work, which in turn motivates the entire class and makes the class much more engaging." | "Professor Ren is the best professor since he was super friendly and he answered all types of questions SUPER QUICK. He lead us to get to the answers if we stuck anywhere. He was super patient to answer the student's questions."*
- **(Spring 2019) CEN 598: Hardware Acceleration and FPGA Computing#** | *Teaching Eval: 4.68 / 5.0*
  Enrollment Size: 66; Some student comments: *"The passion of instructor towards this course is awesome, One of the best Professors I have ever studied from." | "Professor is more informative and gives more insights about the questions asked in the interview." | "I love computer hardware design courses like this! I wish ASU had more. Dr. Ren teaches very well, answers questions with much*

expertise/insight, and makes a good case for in-person classes."

- **(Fall 2018) CEN 598: Hardware Acceleration and FPGA Computing#** | *Teaching Eval: 4.69 / 5.0*
  Enrollment Size: 89; Some student comments: *"Professor communicates his ideas clearly and encourages students to think. The mode of instruction is highly interactive. I believe that is the best quality of teaching that I have had in my entire life as a student and I am extremely happy to be a student under him." | "Very practical and useful course to understand the concepts of digital design from a system level perspective." | "Topics covered are industry oriented and the professor's clarity in explaining concepts is remarkable."*
- **(Fall 2018) CSE 320: Design/Synthesis of Digital Hardware‡** | *Teaching Eval: 4.54 / 5.0*
  Enrollment Size: 66; Some student comments: *"The instructor was always prepared for his lectures and his lectures are always interesting, he makes the materials really easy to understand and he is always open to questions." | "It was very intriguing and the professor did a really good job connecting what we were talking about to how it is used in industry. The instructor was very knowledgeable about the subject matter as well and could go in depth on most topics if the students asked him about it." | "The subject was very interesting and Professor Ren discussed each topic thoroughly. He knew how to engage with students to allow this sort of interaction."*
- **(Spring 2018) CEN 598: Hardware Acceleration and FPGA Computing#** | *Teaching Eval: 4.66 / 5.0*
  Enrollment Size: 92; Some student comments: *"Professor Ren's teaching is clear and comprehensive, the material covers much knowledge that is essential for future research and work. And he is enthusiastic about his teaching." | "The professor has given lot of good material and always comes prepared to class." | "Professor is very contentful and student friendly and always provided lectures which have close relation with real time industrial standards and was always open to doubts and made sure that content is properly conveyed."*
- **(Fall 2017) CEN 598: Hardware Acceleration and FPGA Computing#** | *Teaching Eval: 4.8 / 5.0*
  Enrollment Size: 50; Some student comments: *"The courses is tailored made for state of the art hardware optimization concepts, which is absolutely necessary for any digital design student. Specifically, my research work requires a good understanding of all these concepts, which were taught extremely well in this class." | "Exceptional lectures delivered by Dr. Ren" | "The lectures are very insightful and helped me understand hardware in a new light." | "Prof Ren is amazing teacher and explains the concepts at great depth in a lucid way."| "The course content is awesome. It makes me industry ready fully."*
- **(Fall 2017) CSE 320: Design/Synthesis of Digital Hardware‡** | *Teaching Eval: 4.44 / 5.0*
  Enrollment Size: 69; Some student comments: *"Professor Ren is knowledgeable and accessible, one of the best professors I have met for CSE courses." | "Very knowledge and enthusiastic professor. Made me proud to be getting into computer engineering." | "I always looked forward to the lectures by Professor Ren because he not only explained everything clearly with examples but he was very passionate about the curriculum and that enthusiasm was very contagious for the classroom environment." | "I love the course and lecture...the content is fantastic. Ren is an amazing professor and very passionate/lively."*
- **(Spring 2017) ASU 101-CSE: ASU Experience** | *Teaching Eval: 4.88 / 5.0*
  Enrollment Size: 19; Some student comments: *"What I liked most about this course is the many information about the resources of ASU. I was able to know about the tutoring service, career help, and extra-curricular organizations that are all available at ASU. These resources will help me get comfortable at ASU and prepare for my future career."*
- **(Spring 2017) CEN 598: Hardware Acceleration and FPGA Computing#** | *Teaching Eval: 4.78 / 5.0*

Enrollment Size: 113; Some student comments: *"Good professor. He knows what he is talking about. Always gives chance to the students to talk up." | "The instructor was well prepared, could tie concepts with applications effectively" | "The course is well suited for EEE students. I strongly believe that either this course or at least a part of this course should be made into a compulsory requirement for EEE or incorporated in one of the VLSI courses, as compulsory requirement." | "Great professor, very well organized" | "Fengbo Ren tutored us well with his extensive knowledge and command on this subject." | "I like the way the professor conveys his idea. It clear and profound."*

- **(Fall 2016) CSE 320: Design/Synthesis of Digital Hardware‡** | *Teaching Eval: 4.40 / 5.0*
  Enrollment Size: 50; Some student comments: *"Fengbo was always very prepared and really knew his stuff." | "I really liked the lectures. They were very informative." | "Dr. Ren is a really nice person. He is always willing to spend time helping you." | "The labs were very interesting and occasionally very challenging." | "That the professor would write on a whiteboard, and make sure the students got the concepts."*
- **(Spring 2016) CEN 598: Hardware Acceleration and FPGA Computing#** | *Teaching Eval: 4.72 / 5.0*
  Enrollment Size: 106; Some student comments: *"The professor was well prepared and taught all that is needed in a very clear and concise manner." | "The Faculty had in depth knowledge in the course and taught us well." | "The homework is very well structured and explored many new possibilities." | "New topic which provides excellent future career opportunities" | "The in-depth explanation of the fundamental concepts and its application to the various fields."*
- **(Fall 2015) CSE 320: Design/Synthesis of Digital Hardware‡** | *Teaching Eval: 3.22 / 5.0*
  Enrollment Size: 61; Some student comments: *"The professor does care about the topic. The passion and knowledge is clear to see. He's also ready to help during his office hours, explaining some concepts that weren't clearly explained during the lecture." | "I like the most about the hardware portion of this class and the time we spent doing work in the embedded lab was great pretty much the second half of the semester. Dr. Ren was super knowledgeable and to see him knowing so much about the subject made me want to do better in the class."*

STUDENTS OR TRAINEES MENTORING

Ph.D. Dissertation (Co-)Chaired

8. **Zifan Yu** (Fall 2020-Now, Computer Science, CIDSE, ASU)
   Research Topics: Compressive Learning
7. **Masudul Quraishi** (Fall 2019-Now, Computer Engineering, CIDSE, ASU)
   Research Topics: Reconfigurable High-Performance Computing
6. **Erfan Bank Tavakoli** (Fall 2019-Now, Computer Engineering, CIDSE, ASU)
   Research Topics: Reconfigurable High-Performance Computing
5. **Zhikang Zhang** (Fall 2017-Now, Computer Science, CIDSE, ASU)
   Research Topics: Data-driven Compressive Sensing, Deep Learning
4. **Michael Riera** (Spring 2017-Now, Computer Engineering, CIDSE, ASU)
   Research Topics: Heterogeneous High-Performance Computing
3. **Saman Biookaghazadeh** (Spring 2017-Now, Computer Science, CIDSE, ASU)
   Co-advised with Prof. Ming Zhao
   Research Topics: FPGA-based Acceleration for Big Data Analytics
2. **Yixing Li** (Fall 2015–Spring 2021, Computer Engineering, CIDSE, ASU)
   "Hardware-Friendly Deep Learning for Edge Computing", Ph.D. Dissertation, Computer Engineering, CIDSE, ASU, Chair: Fengbo Ren, Committee Members: Baoxin Li, Sarma Vrudhula, Jae-sun Seo.

1. **Kai Xu** (Summer 2015–Spring 2021, Computer Engineering, CIDSE, ASU)
   "Learning in Compressed Domains", Ph.D. Dissertation, Computer Engineering, CIDSE, ASU, Chair: Fengbo Ren, Committee Members: Baoxin Li, Yezhou Yang, Pavan Turaga.

M.S. Thesis (Co-)Chaired

2. **Akshay Dua** (Summer 2018–Fall 2019, Computer Engineering, ECEE, ASU)
   "OpenCL-based FPGA Acceleration for Real-time Video Analytics on Network Edge", M.S. Thesis, Electrical Engineering, ECEE, ASU, Fall 2019, Chair: Fengbo Ren, Committee Members: Baoxin Li, Sarma Vrudhula.
1. **Aswin Gunavelu Mohan** (Summer 2016–Spring 2017, Electrical Engineering, ECEE, ASU)
   "Hardware Acceleration of Most Apparent Distortion Image Quality Assessment Algorithm on FPGA Using OpenCL", M.S. Thesis, Electrical Engineering, ECEE, ASU, Spring 2017, Co-Chair: Fengbo Ren, Sohum Sohoni, Committee Members: Jae-sun Seo.

Other Graduate Students Advised for Sponsored Research

3. **Aravind Rameshan Thampi** (Summer 2017, Computer Engineering, ECEE, ASU)
   Research Topics: Real-time Compressive Sensing Systems for Wireless ECG Monitoring
2. **Vamsi Krishna Sakalabattula** (Summer 2017, Computer Engineering, ECEE, ASU)
   Research Topics: Real-time Compressive Sensing Systems for Wireless ECG Monitoring
1. **Abhilash Sureshbabu** (Fall 2015–Summer 2016, Electrical Engineering, ECEE, ASU)
   Research Topics: Compressive Sensing Based Sensor SoC for Physiological Monitoring
   RA Support: Fall 2015–Summer 2016

Visiting Scholars

1. **Yuhao Wang** (Fall 2015)
   Ph.D., Nanyang Technological University, Singapore
   Research Topics: Sensing Matrix Binarization, OpenCL-based FPGA Computing

Undergraduate Students Advised for Sponsored Research

10. **Jonathan Zhao** (Fall 2020–Spring 2021, Computer Science, CIDSE ASU)
    Research Project: Open Image Compressive Sensing Toolbox and Benchmark
    NSF REU Support: Fall 2020
9. **Matthew Westerham** (Summer 2020–Fall 2020, Computer Science, CIDSE, ASU)
   Research Project: Evaluation of Data-driven Compressive Sensing Frameworks
   NSF REU Support: Summer and Fall 2020
8. **Mark Lakatos-Toth** (Spring 2020–Fall 2020, Computer Science, CIDSE, ASU)
   Research Project: Evaluation of Data-driven Compressive Sensing Frameworks
   FURI Support: Summer and Fall 2020
   RA Support: Spring 2020
7. **Avi Moskoff** (Spring 2020–Spring 2020, Computer Science and Mathematics, CIDSE, ASU)
   Research Project: Evaluation of Data-driven Compressive Sensing Frameworks
   NSF REU Support: Spring, Summer, and Fall 2020
6. **Raghav Madan** (Summer 2018–Fall 2018, Computer System Engineering, CIDSE, ASU)
   Research Project: IoT and Robotics in Pet Care
   FURI Support: Fall 2018
5. **Sean Slamka** (Spring 2018, Computer Systems Engineering, ECEE, ASU)
   Research Project: Design and Implementation of an Internet-of-Things (IoT) Based Activity Tracker for Pet Care
   FURI Support: Spring 2018

4. **Tae Hun Yun** (Summer 2017–Fall 2017, Computer System Engineering, CIDSE, ASU)
   Research Project: Internet-of-things (IoT) for Pet Care
   RA Support: Summer 2017; FURI Support: Fall 2017
3. **Zhiqian Li** (Summer 2017–Fall 2017, Computer System Engineering, CIDSE, ASU)
   Research Project: Internet-of-things (IoT) for Pet Care
   RA Support: Summer 2017; FURI Support: Fall 2017
2. **Gabriela Coote** (Fall 2016–Spring 2017, Mechanical Engineering, SEMTE, ASU)
   Research Project: Internet-of-things (IoT) for Pet Care
   RA Support: Fall 2016; FURI Support: Spring 2017
1. **Rafeeul Alam** (Fall 2016, Electrical Engineering, ECEE, ASU)
   Research Project: Internet-of-things (IoT) for Pet Care
   RA Support: Fall 2016

Honors Theses (Barrett Honors College)

6. **Ariana Kiaei** (Fall 2020–Spring 2021, Computer Science + Electrical Engineering, CIDSE, ASU)
   "Fido Tracker: A Prototype Solution to Mobile Pet GPS Tracking", Honor Thesis, Barrett, the Honors College, ASU, Spring 2021, Chair: Fengbo Ren, Committee Members: Seth Abraham.
5. **Evan Lam** (Fall 2018–Spring 2019, Computer Systems Engineering, CIDSE, ASU)
   "Exploring the Implementation of Multiple Partial Reconfiguration Regions to use FPGAs in Edge Computing", Honor Thesis, Barrett, the Honors College, ASU, Spring 2019, Chair: Fengbo Ren, Committee Members: Sarma Vrudhula.
4. **Brandon Barth** (Fall 2018–Spring 2019, Computer Systems Engineering, CIDSE, ASU)
   "FPGAs as an Edge Computing Solution", Honor Thesis, Barrett, the Honors College, ASU, Spring 2019, Chair: Fengbo Ren, Committee Members: Sarma Vrudhula.
3. **Cody Gillespie** (Fall 2018–Spring 2019, Computer Science, CIDSE, ASU)
   "An IoT Solution for Air Quality Monitoring", Honor Thesis, Barrett, the Honors College, ASU, Spring 2019, Chair: Fengbo Ren, Committee Members: Aviral Shrivastava.
2. **Abrahm Coury** (Fall 2018–Spring 2019, Computer Science, CIDSE, ASU)
   "An IoT Solution for Air Quality Monitoring", Honor Thesis, Barrett, the Honors College, ASU, Spring 2019, Chair: Fengbo Ren, Committee Members: Aviral Shrivastava.
1. **Gabriela Coote** (Fall 2016–Spring 2017, Mechanical Engineering, SEMTE, ASU)
   "Internet-of- Things for Pet Care", Honor Thesis, Barrett, the Honors College, ASU, Spring 2017, Chair: Fengbo Ren, Committee Members: Aviral Shrivastava.

ASU Ph.D. Dissertation Committee

5. **Alham Azari**, "Reduced Order Models and Approximations for Hardware Acceleration of Neural Networks", Ph. D. Dissertation, Computer Engineering, CIDSE, ASU, Spring 2021, Chair: Sarma Vrudhula, Committee Members: Georgios Fainekos, Fengbo Ren, Yezhou Yang.
4. **Ron Jokai**, "Efficient Reconfigurable Computing in Radiation-Susceptible Environments", Ph. D. Dissertation, Electrical Engineering, ECEE, ASU, Summer 2020, Chair: John Brunhaver, Committee Members: Lawrence Clark, Jae-sun Seo, Fengbo Ren.
3. **Jinane I. Mounsef**, "Distortion Robust Biometric Recognition", Ph. D. Dissertation, Electrical Engineering, ECEE, ASU, Fall 2018, Chair: Lina Karam, Committee Members: Baoxin Li, Fengbo Ren, Antonia Papandreou-Suppappola.
2. **Jian Cai**, "Scratchpad Management in Software Managed Manycore Architectures", Ph.D. Dissertation, Computer Science, CIDSE, ASU, Fall 2017, Chair: Aviral Shrivastava, Committee: Fengbo Ren, Partha Dasgupta, Carole-Jean Wu.

1. **Shin-Ying Lee**, "Dynamic Warp Scheduling and Intelligent Cache Management Techniques for Modern GPU Architectures", Ph.D. Dissertation, Computer Engineering, CIDSE, ASU, Fall 2017, Chair: Carole-Jean Wu, Committee: Fengbo Ren, Chaitali Chakrabarti, Aviral Shrivastava.

ASU M.S. Thesis & Applied Project Committee

9. **Pravin Kumar Ravi**, "FPGA acceleration of CNNs using OpenCL", M.S. Thesis, Computer Science, CIDSE, ASU, Jul. 2020, Chair: Ming Zhao, Committee: Baoxin Li, Fengbo Ren.
8. **Harshith Allamsetti**, "Cooperative Driving of Connected Autonomous Vehicles Using Responsibility Sensitive Safety Rules", M.S. Thesis, Computer Engineering, CIDSE, ASU, Jun. 2020, Chair: Aviral Shrivastava, Committee: Fengbo Ren, Arunabha Sen.
7. **Saurabh Animesh**, "Algorithm Architecture Co-Design for Dense and Sparse Matrix Computations", M.S. Thesis, Electrical Engineering, ECEE, ASU, Nov. 2018, Chair: Chaitali Chakrabarti, Committee: Fengbo Ren, John Brunhaver.
6. **Jinn-Pean Lin**, "Optimizing Heap Data Managemention Software Managed Manycore Architectures", M.S. Thesis, Computer Science, CIDSE, ASU, Jun. 2017, Chair: Aviral Shrivastava, Committee: Fengbo Ren, Umit Ogras.
5. **Vignesh Kannan**, "An Analysis of the Memory Bottleneck and Cache Performance of Most Apparent Distortion Image Quality Assessment Algorithm on GPU", M.S. Thesis, Electrical Engineering, ECEE, ASU, Nov. 2016, Chair: Sohum Sohoni, Committee: Fengbo Ren, Mohamed Sayeed.
4. **Pranay Reddy Gankidi**: "FPGA Accelerator Architecture for Q Learning and Its Applications in Space Exploration Rovers", M.S. Thesis, Computer Engineering (Electrical Engineering), ECEE, ASU, Nov. 2016, Chair: Jekanthan Thangavelautham, Committee: Fengbo Ren, Jae-sun Seo.
3. **Shail J. Dave**: "Scalable Register File Architecture for CGRA Accelerators", M.S. Thesis, Computer Engineering (Electrical Engineering), ECEE, ASU, Nov. 2016, Chair: Aviral Shrivastava, Committee: **Fengbo Ren**, Umit Ogras.
2. **Saktiswarup Satapathy**: "Data Path Implementation for A Spatially Programmable Architecture Customized for Image Processing Applications", M.S. Thesis, Computer Engineering (Computer Systems), CIDSE, ASU, Jun. 2016, Chair: John Brunhaver, Committee: Fengbo Ren, Lawrence Clark.
1. **Jay Patel**: "Dynamic Analysis of Multi-threaded Embedded Software to Expose Atomicity Violations", M.S. Thesis, Computer Engineering (Computer Systems), CIDSE, ASU, Mar. 2016, Chair: Yann-Hang Lee, Committee: Fengbo Ren, Aviral Shrivastava.

High-School Teachers

2. **Deborah Lenz** (Summer 2019, High-School Teacher Training Program Participant)
   Chemistry Teacher, McClintock High School, Tempe, AZ
   Under Dr. Ren's guidance, Mrs. Lenz learned about and refine the laboratory course modules developed in the previous years. The refined course modules were implemented across two sessions of Mrs. Lenz's advanced chemistry class in the Fall 2019 semester, which has reached out to a total of ***42*** gifted students in McClintock High School, Tempe, AZ, to impart them with hands-on hardware and software development experience as well as share the excitement of engineering research.
1. **Matthew Prater** (Summer 2017 and Summer 2018, High-School Teacher Training Program Participant)
   Chemistry/STEM Teacher, Highland High School, Gilbert, AZ
   Under Dr. Ren's guidance, Mr. Prater developed a laboratory course module for high-school students to build an IoT-based temperature sensor from scratch for studying the thermodynamic model of heat transfer for Metal as well as a laboratory course module for high-school students to build an IoT-based digital scale from scratch for learning about mass and weight. The developed

course modules were implemented across multiple sessions of Mr. Prater's chemistry class in the Fall 2017, Spring and Fall 2018 semesters which has reached out to a total of ***267*** students in Highland High School, Gilbert, AZ, to impart them with hands-on hardware and software development experience as well as share the excitement of engineering research.

HONORS AND AWARDS

Faculty Honors and Awards

- IEEE Senior Member, 2020
- ACM Senior Member, 2020
- Fulton Schools of Engineering Best Teacher Award - Top 5%, ASU, 2018-2019
- Fulton Schools of Engineering Best Teacher Award - Top 5%, ASU, 2017-2018
- Google Faculty Research Award, 2018
- Fulton Schools of Engineering Best Teacher Award - Top 5%, ASU, 2016-2017
- NSF Faculty Early Career Development (CAREER) Award, 2017
- Broadcom-UCLA Fellow, Broadcom Inc. and UCLA, 2012
- Graduate Division Fellowship, UCLA, 2011-2012
- Best Performance in Ph.D. Preliminary Examination, ranked No. 1 out of 21 candidates in the Circuit and System area, UCLA, 2010

PhD Student Honors and Awards

- Masudul Hassan Quraishi, Outstanding Computer Engineering (CS) TA Award, CIDSE, ASU, 2020-2021
- Kai Xu, Outstanding Computer Engineering (CS) PhD Student Award, CIDSE, ASU, 2020-2021
- Yixing Li, CIDSE Doctoral Fellowship, ASU, Spring 2020
- Kai Xu, Graduate College Completion Fellowship, ASU, 2019-2020
- Kai Xu, CIDSE Doctoral Fellowship, ASU, Spring 2019
- Yixing Li, CIDSE Doctoral Fellowship, ASU, Spring 2019
- Yixing Li, Student Travel Award, AAAI Conference on Artificial Intelligence, 2018
- Yixing Li, Outstanding Computer Engineering (CS) TA Award, CIDSE, ASU, 2016-2017

IN THE NEWS

- ASU Now, Apr. 28th, 2017:" ASU wins record 14 NSF career awards" by Terry Grant. [link]
- EurekAlert! Science News, Apr. 27th, 2017: "Arizona State University wins record 14 NSF career awards" by Theresa Grant. [link]
- ASU Full Circle, Mar. 20th, 2017: "Ren's Career Award Confronts Energy Limitations Facing Internet of Things" by Pete Zrioka. [link]
- The Arizona Republic, May 14th, 2017: "Home to the Nation's Leading Faculty" by ASU, Section 24A.

SERVICE AND PROFESSIONAL ACTIVITIES

ASU Internal Service

- **2019–2021:**
  - *Member*, Computer Engineering (CEN) Graduate Program Committee
- **2017–2019:**
  - *Chair*, Computer System Engineering (CSE) Undergraduate Program Committee
- **2015–2016:**
  - *Member*, Computer Engineering (CEN) Graduate Program Committee

- *Member*, Human-Centered Computing Faculty Search Committee

Professional Society Service

- **IEEE Circuits and Systems Society**
  - *Member*, Digital Signal Processing Technical Committee, 2016-Now
  - *Member*, VLSI Systems & Applications Technical Committee, 2016-Now

Editorial Service for Peer-reviewed Journals

- **2019:**
  - *Guest Editor*, IEEE Transactions on Biomedical Circuits and Systems (TBioCAS), Special Issue on AI-based Biomedical Circuits and Systems

Conference Service

- **2021:**
  - *Review Committee Member*, IEEE International Symposium on Circuits and Systems (ISCAS)
  - *Session Chair*, Programmable, Reconfigurable & Array Architectures; Digital Circuits, Systems & Architectures for Machine Learning I, International Symposium on Circuits and Systems (ISCAS)
  - *Review Committee Member,* The 3rd IEEE International Conference on Artificial Intelligence Circuits and Systems (AICAS)
- **2020:**
  - *Program Committee Member,* The 3rd USENIX Workshop on Hot Topics in Edge Computing (HotEdge)
  - *Review Committee Member*, IEEE International Symposium on Circuits and Systems (ISCAS)
  - *Session Chair*, Digital Signal Processing Circuits; Digital Circuits, Systems & Architectures for Machine Learning I, International Symposium on Circuits and Systems (ISCAS)
  - *Review Committee Member,* The 2nd IEEE International Conference on Artificial Intelligence Circuits and Systems (AICAS)
- **2019:**
  - *Track Chair*, Emerging and Evolutionary Design, The 32nd IEEE International System-on-Chip Conference (SOCC)
  - *Review Committee Member*, IEEE International Symposium on Circuits and Systems (ISCAS)
  - *Session Chair*, DSP Systems/Applications; Energy-Aware Computing & 3D ICs, International Symposium on Circuits and Systems (ISCAS)
  - *Technical Committee Member,* Signal Image and Video Processing Architectures, The 26th IEEE International Conference on Electronics Circuits and Systems (ICECS)
- **2018:**
  - *Local Chair*, The 27th International Symposium on High-Performance Parallel and Distributed Computing (HPDC)
  - *Technical Committee Member*, Signal Image and Video Processing Architectures, The 25th IEEE International Conference on Electronics Circuits and Systems (ICECS)
- **2017:**
  - *Review Committee Member*, IEEE International Symposium on Circuits and Systems (ISCAS)
  - *Session Chair*, Low-power Digital Circuits, International Symposium on Circuits and Systems (ISCAS)
- **2015:**
  - *Technical Program Committee Member*, IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC)

Proposal Review Service

National Science Foundation

- SBIR/STTR Program (Artificial Intelligence), 2020

Reviewer for Journals

- IEEE Transactions on Industrial Electronics (TIE)
- IEEE Internet of Things Journal
- IEEE Transactions on Smart Grid (TSG)
- IEEE Journal of Solid-State Circuits (JSSC)
- IEEE Transactions on Electron Devices (TED)
- IEEE Transactions on Nanotechnology (TNANO)
- IEEE Transactions on Circuits and Systems I: Regular Papers (TCAS-I)
- IEEE Transactions on Circuits and Systems II: Express Briefs (TCAS-II)
- IEEE Transactions on Very Large Scale Integration Systems (TVLSI)
- IEEE Transactions on Biomedical Circuits and Systems (TBioCAS)
- IEEE Transactions on Magnetics (TMAG)
- IEEE Systems Journal (SJ)
- IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)
- IEEE Signal Processing Letters (SPL)
- IEEE Consumer Electronics Magazine
- Journal of Neuroscience Methods
- Signal Processing: Image Communication
- PLOS ONE
- Circuits, Systems & Signal Processing
- Journal of Semiconductors
- Canadian Journal of Electrical and Computer Engineering
- SPIN

Reviewer for Conferences

- IEEE International System-on-Chip Conference (SOCC), 2019
- IEEE International Symposium on Bioelectronics and Bioinformatics (ISBB), 2014-2015
- IEEE/CAS-EMB Biomedical Circuits and Systems Conference (BioCAS), 2015
- International Symposium on Integrated Circuits (ISIC), 2014
- IEEE International Symposium on Circuits and Systems (ISCAS), 2013-2014
- IEEE International Conference on Computer & Communication Technology (ICCCT), 2011-2012

Professional Memberships

Senior Member, Institute of Electrical and Electronics Engineers (IEEE): S'10-14, M'14-20, SM'20-now

- IEEE Solid-State Circuits Society
- IEEE Circuits and Systems Society
- IEEE Signal Processing Society
- IEEE Computer Society

Member, Association for Computing Machinery (ACM): M'14-20, SM'20-now

- Special Interest Group on Embedded Systems (SIGBED)
- Special Interest Group on High Performance Computing (SIGHPC)
- Special Interest Group on Artificial Intelligence (SIGAI)