# True Energy-Performance Analysis of the MTJ-Based Logic-in-Memory Architecture (1-Bit Full Adder)

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***Abstract*—The use of spin-transfer torque (STT) devices for memory design has been a subject of research since the discovery of the STT on MgO-based magnetic tunnel junctions (MTJs). Recently, MTJ-based computing architectures such as logic-in-memory have been proposed and claim superior energy-delay performance over static CMOS. In this paper, we conduct exhaustive energy-performance analysis of an STT-MTJ-based logic-in-memory (LIM-MTJ) 1-bit full adder and compare it with its corresponding CMOS counterpart. Our results show that the LIM-MTJ circuit has no advantage in energy-performance over its equivalent CMOS designs. We also show that the MTJ-based logic circuit requiring frequent MTJ switching during the operation is hardly power efficient.**

***Index Terms*—Adders, complimentary metal–oxide–semiconductor (CMOS) digital integrated circuits, energy-delay tradeoff, magnetic tunnel junction (MTJ) logic, spin-transfer torque (STT) devices.**

## I. Introduction

EVOLUTIONARY device scaling of CMOS technology to nanometer-scale technology nodes below $< 22$ nm has resulted in physical constraints leading to very high device leakage and performance instability that greatly deteriorate CMOS performance and functionality. The high leakage can cause loss of information during unexpected power supply interruptions (volatility). In particular, the exponential nature of CMOS standby power consumption creates difficulty in implementing designs for low-power applications.

To extend the scaling and reduce energy dissipation for ultra-low-power applications, various emerging devices have been suggested in the International Technology Roadmap for Semiconductors [1]. However, CMOS technology will continue to march to the next decade and lead technology innovations despite its increasing scaling problems [1]. Thus, in a short term, people will keep looking for new switches that supplement CMOS, are CMOS compatible, and can support ultra-low-power operation. Spin-based devices are among the candidates for these goals, as the energy needed to change an electron spin is a minute fraction of what is needed to move the electronic charge [2].

Magnetic tunnel junction (MTJ) is one of the most basic and also most significant spin-based devices. The discovery of the spin-transfer torque (STT) phenomenon renders MTJ-based magnetic random access memory to be considered a strong candidate for universal memory [3], [4]. Since any memory could be used to build a logic circuit, at least in theory, the MTJ is no exception as it has a relatively high tunnel magnetoresistance (TMR) ratio, which keeps getting improved with the invention of MgO as the tunneling barrier [5]. The MTJ is also CMOS-compatible with high stability, reliability, and nonvolatility [6]. In addition, the STT-MTJ can be fabricated on top of CMOS devices to reduce the area cost [7]. All these features give hope to building a nonvolatile logic circuit that does not consume OFF-state leakage current and supports ultra-low-power operation.

So far, several MTJ-based computing architectures have been proposed. These proposals have been able to use 1) the magnetic field interaction generated by the input line passing through the MTJ element to change the magnetization of a free layer to implement logic [7]; 2) a sense amplifier to read the total resistance difference between two groups of the MTJ's stack determined by inputs to implement logic [9]–[11]; and 3) the MTJ as a memory cell and a CMOS as a control circuit to conduct writing and reading operations (to implement a flip-flop) [11], [12]. However, almost all of the above proposals on MTJ-based computing architectures are conceptual, with rare energy and performance analysis. There is only one paper [7] that reports power and performance comparisons to CMOS implementation for an adder design. The paper claims that a logic-in-memory MTJ (LIM-MTJ) 1-bit full adder has both lower dynamic and static power than a static CMOS (SCMOS). The study omits dynamic CMOS implementation, considers only one point in the energy-delay space, and does not include time and energy for writing an MTJ cell.

In this paper, we conduct a comprehensive energy and performance analysis of the LIM-MTJ architecture by plotting the energy-delay curve (EDC) of an LIM-MTJ 1-bit full adder and comparing it with both static and dynamic CMOS designs. The comparisons with 180-, 90-, and 65-nm predictive technology models (PTMs) in HSPICE will be made to project scaling trends. The simulation results show that the LIM-MTJ architecture has no advantage in energy-performance over its equivalent CMOS design. It will be shown that the use of the MTJ deteriorates the energy-delay tradeoff. Finally, we will

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show that, with the devices analyzed, the MTJ-based logic requiring frequent MTJ switching is hardly power efficient due to a high writing energy of the MTJ as compared with the CMOS switching energy.

The organization of this paper is as follows. Section II presents the MTJ structure and its writing method, and the architecture of two logic styles that we compared, i.e., the LIM-MTJ and dynamic current-mode logic (DyCML). In Section III, our analysis, comparison methods, and simulation settings are described. Discussions of simulation results based on energy-delay plots for various 1-bit full adder implementations and the analyzed MTJ writing energy are provided in Section IV. Section V concludes this paper.

## II. Device and Circuit Architecture

### A. MTJ Stack

An MTJ is composed of two layers of a ferromagnetic material (a fixed layer and a free layer) separated by an extremely thin nonconductive tunneling (MgO, $Al_2O_3$, etc.) barrier (Fig. 1). The MTJ resistance depends on the relative orientation of the magnetization directions of the two ferromagnetic layers due to spin-dependent tunneling involved in the electron transport between the majority and minority spin states. If the spin orientations are parallel, applying a voltage across the MTJ is more likely to cause electrons to tunnel through the thin barrier without being strongly scattered, resulting in high current flow and low resistance $(R_P)$. In contrast, the resistance is high $(R_{\rm AP})$ if the spin orientations are antiparallel. The resistance change is measured by a TMR ratio, which is defined as $\Delta R/R = (R_{\rm AP} - R_P)/R_P$. With the MgO oxide barrier, the TMR ratio could reach 500% at room temperature and 1010% at 5 K [6]. Most practical devices have TMR ratios between 50% and 150%. The write operation can be done by flipping the magnetization direction of the free layer (the fixed layer cannot be changed) with a spin-polarized current (Fig. 1). The current density through the STT needs to be higher than the critical current density $J_C$ to flip the magnetization direction [14]. Reverse current direction results in the reverse magnetization direction of the free layer and, consequently, different resistance (Fig. 1). The read operation is done by measuring the spin-dependent tunneling current (resistance change) between the magnetic layers. This device is scalable because the absolute writing current scales with the junction size assuming that $J_C$ is independent on the MTJ size [6].

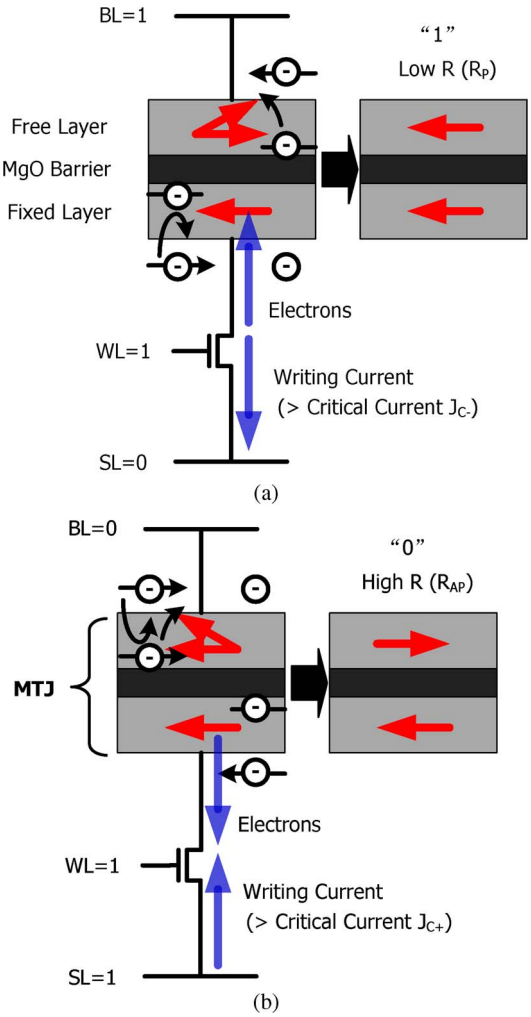


Fig. 1. Illustration of the MTJ and the writing operation using the STT. (a) Writing MTJ from antiparallel (0) to parallel (1). (b) Writing MTJ from parallel (1) to antiparallel (0).

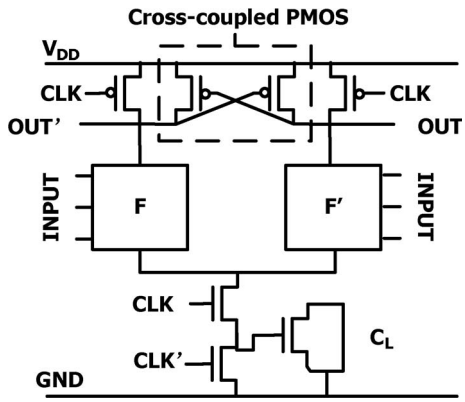


Fig. 2. Structure of the DyCML logic.

### B. DyCML Style

DyCML circuits combine the advantages of metal–oxide–semiconductor current-mode logic circuits with those of dynamic logic families to achieve high performance at a low voltage swing and low power dissipation [15]. Fig. 2 shows the general structure of the DyCML logic. A function $F$ is implemented using two pull-down networks that implement $F$ and $F'$. Either $F$ or $F'$ will turn on to evaluate the logic output. During the precharge phase $(\text{CLK} = 0)$, both outputs are precharged to "1," and the capacitance transistor $C_L$ is fully discharged. During the evaluation phase $(\text{CLK} = 1)$, the pull-down network with low resistance will discharge its output to "0" and turn on the cross-coupled PMOS transistor in the opposite branch to compensate the leakage and charge its output to stay at "1." As a result, the voltage levels of the two outputs are separated and become complementary. $C_L$ serves as a virtual ground during the evaluation phase and eliminates static power. Thus, by adjusting the width of the $C_L$ transistor, the voltage swing can be controlled, allowing the circuit to trade off between speed and power consumption.

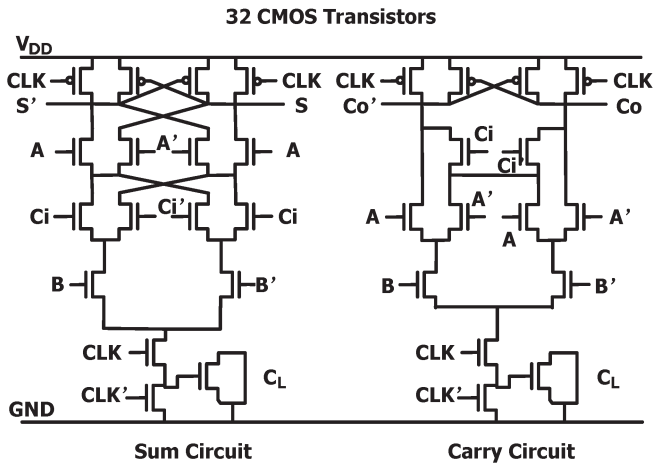


Fig. 3. Schematic of the DyCML 1-bit full adder.

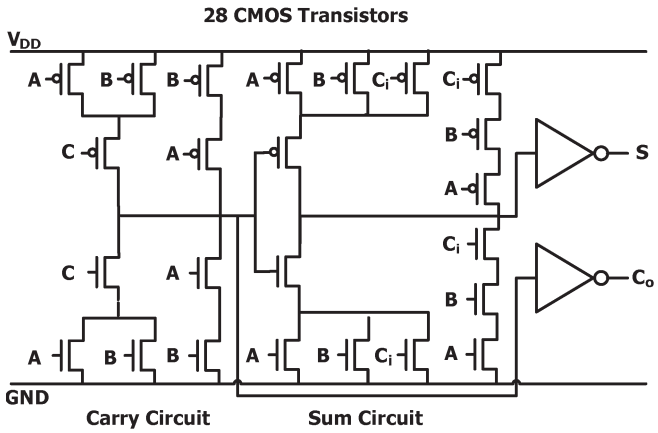


Fig. 4. Schematic of the SCMOS 1-bit full adder implemented in a mirror structure.

A 1-bit full adder implemented with the DyCML circuit is shown in Fig. 3. It consists of 32 transistors as compared with 28 transistors in an SCMOS realization shown in Fig. 4.

### C. LIM-MTJ Logic Style

Fig. 5 shows a general structure of the LIM-MTJ logic. For a function $F$, two logic networks are constructed by MTJs and CMOS transistors to satisfy that $R(X,Y) < R'(X,Y)$ when $F = 0$ and $R(X,Y) > R(X,Y)'$ when $F = 1$ [16]. The current comparator is used to sense the current difference (resistance difference) of the two pull-down networks. If $I > I'$, $Z = 0$, else if $I < I'$, $Z = 1$. The LIM-MTJ logic is implemented by using the DyCML structure (Fig. 2). The only difference between the LIM-MTJ and the DyCML is that the pull-dow network in the LIM-MTJ has MTJs that serve both as memory and functional inputs, in addition to having regular CMOS transistors in the pull-down network. Thus, the LIM-MTJ can be considered as an MTJ-based DyCML.

Fig. 6 shows a 1-bit full adder implemented with the LIM-MTJ circuit. It consists of 34 CMOS transistors (26 for logic, 8 for MTJ writing) and 4 MTJs. The use of MTJs cuts down the number of logic transistors to 26, but another 8 transistors are used to conduct MTJ writing, giving no advantage in the transistor count. The MTJs are used as complementary-stored inputs ($B$ and $B'$). $R_{\rm AP}$ represents "0," and $R_P$ represents "1."

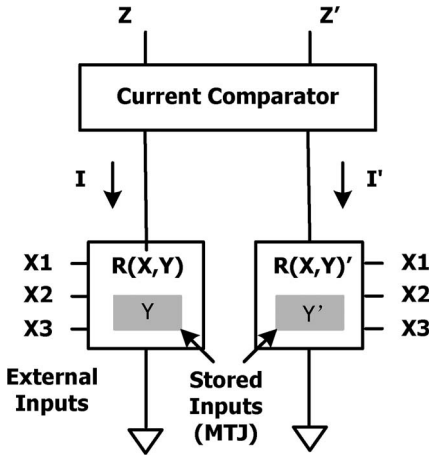


Fig. 5. Structure of the LIM-MTJ logic.

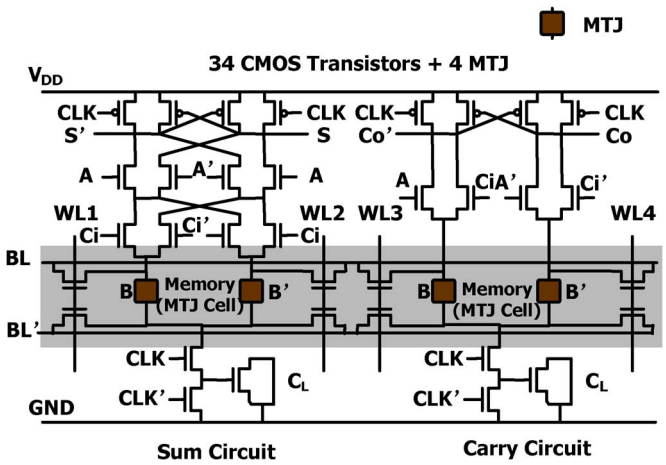


Fig. 6. Schematic of the LIM-MTJ 1-bit full adder.

The $B$ and $B'$ inputs are written via the STT by the transistors shown in the shaded area and controlled by external word-line (WL) and bit-line (BL) signals. The writing transistors are upsized to make sure that they can provide enough current (density $> J_C$) to the MTJ for flipping the magnetic state. Other transistors are sized to ensure that they do not flip the MTJ while the circuit is in the evaluation mode. To best utilize the nonvolatility feature of the MTJ, the stored input should always be the input that is most infrequently changed, which is presumed to be the most significant bit of the circuit in a 2's complement arithmetic.

Fig. 7 shows an example of the switching waveform of an LIM-MTJ 1-bit full adder. In this example, clock is running at 100 MHz, and the voltage swing is $V_{\rm DD}/2$. For certain input vectors (for example, $A = 1$, $B = 1$, $C_i = 1$), both pull-down networks in the sum circuit will have relatively low resistance that differs by $R_{\rm AP} - R_P$. Thus, both networks will drive at the beginning of the evaluation phase; however, the branch with $B = 1$ $(R_P)$ will drive faster and turn on the cross-coupled PMOS of the $B'$ branch to prevent its output $(= 1)$ from pulling down. This fighting process results in the glitches on $S$ and $C_0$ as shown in the waveform (Fig. 7). Since outputs are usually served as inputs of the next stage, this glitch (the voltage drop of output "1" at the beginning of the evaluation phase) is unwanted and will cause bad performance or even

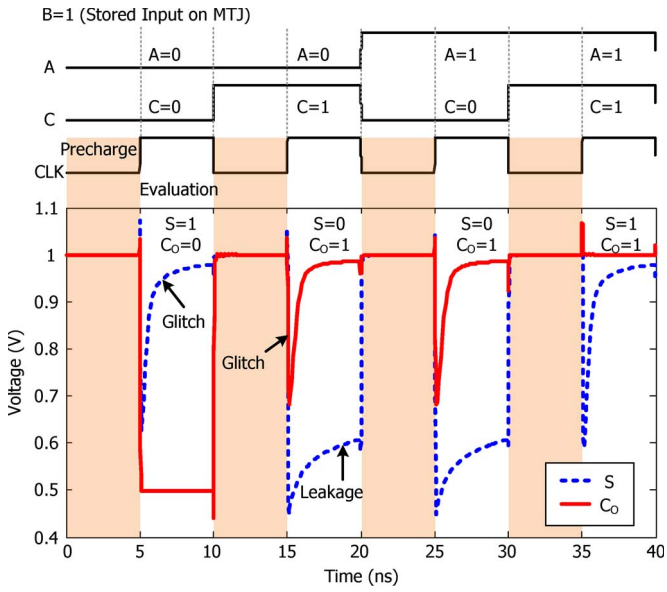


Fig. 7. Switching waveform of the LIM-MTJ 1-bit full adder. The data are from HSPICE simulation with a 90-nm predictive technology model.

incorrect operation of the next stage. The voltage drop depends on both the absolute resistance of the pull-down network (with output "1") and the resistance difference. The higher the resistance and the resistance difference, the smaller the voltage drop. Also, signal degradation of $S$ caused by leakage can be observed from the waveform (Fig. 7) for certain input vectors. The leakage is caused by the direct current through the cross-coupled PMOS and the pull-down network with higher resistance. A device with a higher TMR ratio would reduce the amount of leakage.

## III. Energy-Delay Comparison Method

### A. Energy-Delay Curve (EDC)

To evaluate potential improvements in performance and energy provided by new devices, we plot the EDC for various circuit functions and compare designs in new device technology with those in CMOS. The EDC is plotted by tuning variables in circuits such as transistor size, supply, and threshold voltage. As shown in Fig. 8, the EDC is plotted with time-per-operation versus energy-per-operation. This plot not only shows the best performance and lowest energy design points but also indicates the best energy-delay tradeoff that can be achieved. According to [17], the EDC is defined as a set of optimal design points where the sensitivity of all design variables is equal. Here, the sensitivity is defined as given by

$$S_A(A_0) = \left.\frac{\partial E/\partial A}{\partial D/\partial A}\right|_{A=A_0}, \tag{1}$$

where $E$ is energy, $D$ is delay, and $A$ is a tuning parameter such as transistor size, supply, and threshold voltage. Thus, the solid line in Fig. 8 shows the optimal EDC that we can achieve with a certain circuit topology and device. All design points in the region above the solid line are suboptimal, while the ones below are infeasible. The EDC plot is limited by a minimum-delay point (MDP) and a minimum-energy point (MEP), where

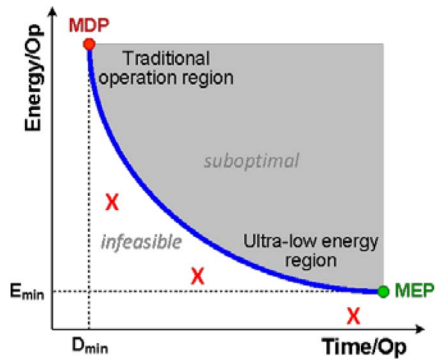


Fig. 8. Illustration of the energy-delay tradeoff in logic circuits.

usually one variable hits its upper or lower bound (e.g., $V_{\rm DD}$ is at the upper bound at the MDP). From the circuit point of view, our goal of investigating the suitability of new devices is to find circuit implementations that operate at points marked as "$X$." We expect eventual "$X$" points below the solid line of CMOS designs more likely to be in the lower power region below the MEP than in the high-performance region beyond the MDP. This is because one of the premises of the new device technologies is to alleviate the leakage problem of CMOS.

### B. Simulation Setup

There are three design variables to consider at the circuit level: supply voltage, gate size, and threshold voltage. Previous work [17] has shown that with less than 25% delay increase from the MDP, sizing is the most efficient way to reduce energy. With more than 25% delay increase, $V_{\rm DD}$ scaling is the most efficient way to reduce energy [17]. Thus, the EDC in the ultra-low-energy region (that is of interest to us) could be quickly estimated by simply sweeping $V_{\rm DD}$.

Since the LIM-MTJ can be regarded as an MTJ-based DyCML, its real CMOS counterpart should be the DyCML and not the SCMOS. Therefore, in this paper, the EDCs of the LIM-MTJ, DyCML, and SCMOS 1-bit full adders are compared in HSPICE using PTM models. To get insight into scaling trends, each EDC is plotted by scaling $V_{\rm DD}$ using 180-, 90-, and 65-nm PTM models, respectively. The capacitance transistor of the LIM-MTJ is sized to achieve a voltage swing of about 50% $V_{\rm DD}$, which assures the cross-coupled PMOS to be fully turned on to stop the pull-down network from discharging the output "1." For a fair comparison, all three adders are loaded with a fan-out-4 output load; the LIM-MTJ and the DyCML are designed for the same voltage swing of 50% $V_{\rm DD}$ as compared with a full voltage swing in the SCMOS. For the lowest possible energy of the LIM-MTJ, the stored input is prewritten into the MTJ as a constant value and assumed static during the energy-delay simulations. We assume $R_P = 1250\,\Omega$ and TMR $= 100\%$ for the MTJ as in [7]. The Energy/Op information for each adder is extracted from the waveform (Fig. 7) by measuring the total energy $E_{\rm tot}$ over a time interval in which eight operations are performed. The energy is calculated as Energy/Op $= E_{\rm tot}/8$. The Delay/Op information is extracted by measuring the worst-case delay of $V_{\rm DD} - V_{\rm swing}/2$ switching between the input and the output on the critical path for the LIM-MTJ and the DyCML, as

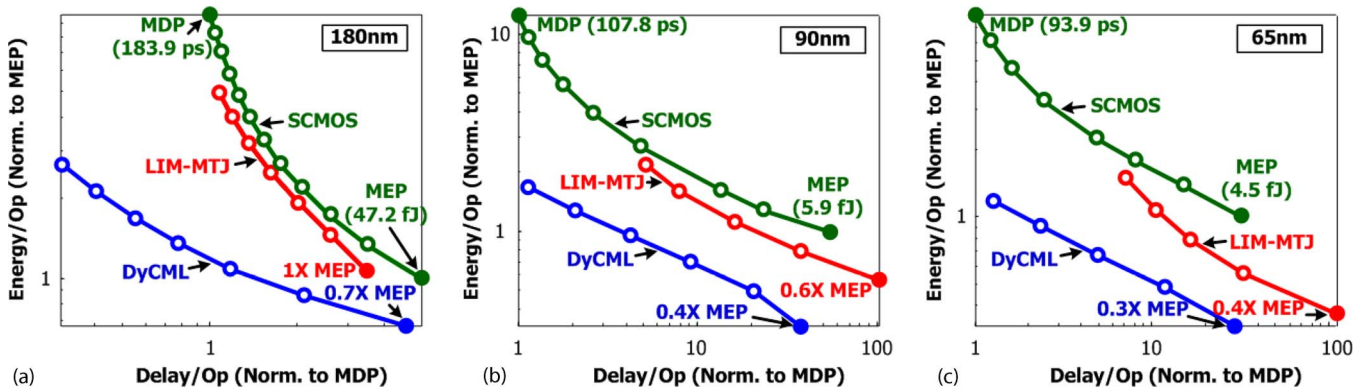


Fig. 9. Energy-delay comparison of 1-bit adder implementations in SCMOS, DyCML, and LIM-MTJ logic styles with (a) 180-nm, (b) 90-nm, and (c) 65-nm models.

compared with $V_{\rm DD}/2$ switching for the SCMOS. Also, the writing energy of the MTJ is analyzed and discussed.

## IV. Simulation Results and Discussion

### A. Energy-Delay Comparison

Fig. 9 shows the EDC results obtained via $V_{\rm DD}$ scaling. The plots are normalized to the MEP and the MDP of the SCMOS design. The results across all technology nodes indicate the same trend. Both the LIM-MTJ and the DyCML are better than the SCMOS in the energy-delay space. For a 180-nm technology, the DyCML achieves 10× higher performance than the SCMOS, while the LIM-MTJ is about the same as the SCMOS. For a 65-nm design, both the DyCML and the LIM-MTJ can achieve 3× energy reduction as compared with the SCMOS. It is interesting that both the LIM-MTJ and the DyCML comparatively lose speed but gain energy reduction with technology scaling. The relative speed degradation makes sense as we move away from using dynamic logic in high-performance designs today. However, it is important to underscore that the DyCML always has better energy-delay tradeoff than the LIM-MTJ, not even considering energy to switch MTJ inputs. This clearly renders the LIM-MTJ suboptimal and impractical.

### B. Including the Writing Energy of the MTJ

The plots in Fig. 9 only show the best-case energy of the LIM-MTJ, in which the input stored on the MTJ is assumed a constant, and no switching energy (or delay) of the MTJ is included. This essentially means an activity factor of zero, which is unrealistic in digital logic. The MTJ switching energy, thus, needs to be included in energy estimates for any practical operation.

The writing energy $E_W$ of the STT-MTJ is defined as the energy dissipated as heat on the MTJ while a switching current $I_W$ flows through the MTJ stack. This energy is given as

$$E_W = I_W^2 \cdot R \cdot t\,, \tag{2}$$

where $I_W$ can be calculated as the product of the MTJ critical current density $J_C$ and the MTJ cross-sectional junction size $A$, $I_W = J_C \cdot A$. The resistance $R$ of the MTJ is calculated using the $RA$ product $\delta$, i.e., $R = \delta/A$. The parameter $t$ is the switching time.

Thus, $E_W$ can also be expressed as

$$E_W = J_C^2 \cdot \delta \cdot A \cdot t. \tag{3}$$

Equation (3) indicates that the writing energy scales quadratically with the current density and is proportional to the $RA$ product $\delta$, the cross-sectional junction area $A$, and the switching time $t$. All of these parameters have been improving toward lower $E_W$ since the first demonstration of STT switching in MTJs in 2004. The first column in Table 1 summarizes the range of each parameter reported in existing references.

TABLE I
Parameters and Writing Energy of the MTJ Reported in [4]–[7], [12], [14], [16], and [18]–[20] and Future Expectation

| | Reported in Ref. | Expected in the Future |
|---|---|---|
| $J_C$ (MA/cm$^2$) | 1-20 | 0.5-1 |
| $\delta$ ($\Omega\mu$m$^2$) | 20-144 | 1-3 |
| A ($\mu$m$^2$) | 0.015-0.03 | 0.0002-0.001 [1] |
| t | 2ns-1s | 1-2ns |
| $E_W$ (fJ) | >100 | <1 |

The minimum writing energy reported is found to be on the order of hundreds of femtojoules. Circuit simulations show that the CMOS energy per operation is on the order of a few femtojoules and is limited by subthreshold leakage. This means the energy used to switch 1 bit of MTJ data is about two orders-of-magnitude larger than the switching energy of a CMOS gate. Considering the energy dissipated on the transistor stack due to the MTJ writing current and the fact that practical switching current is usually 2–4× larger than the critical current $I_W$, the practical writing energy should be even higher, i.e., about 0.5 pJ. As a result, with the writing energy of the MTJ considered, it turns out that the MTJ-based logic circuit requiring frequent MTJ switching is hardly power efficient. This has to be taken cautiously, of course, since the MTJ technology is still in early development stages.

A significant decrease in each parameter in the $E_W$ formula is needed to make the MTJ-based logic competitive with CMOS. The second column in Table I shows the range of each parameter expected in the future given the MTJ writing energy of $< 1$ fJ. Considering that the MTJ switching time below 3 ns will cause a large increase in current density [20], further

reduction of switching time is not practical since it would degrade power efficiency. A current density of 0.5–1 MA/cm$^2$ is doable in a 90-nm CMOS (1 mA/$\mu$m of gate width) [6], [20]; the scaling trend of the writing current density should be always compatible with that of a CMOS transistor. Thus, further improvement on the $RA$ product and the junction size is expected to decrease the writing energy of the MTJ to the femtojoule level. Scale factors of 0.1 on the $RA$ product and 0.01 on the junction size are expected in the future (Table I). Such a scaled device would be very compelling for integration with CMOS for a variety of applications.

Other components of energy also have to be evaluated. In CMOS, for example, the dynamic energy is becoming a smaller portion of the overall energy in presence of leakage and interconnect energy. The higher density of MTJ-assisted CMOS logic could address the interconnect energy, for example. More elaborate MTJ parameters and scaling trends are needed for complete evaluation of these effects.

## V. Conclusion

The LIM-MTJ has no advantage in energy-performance over its equivalent CMOS design. Due to the high leakage current caused by the relatively small $R_{\mathrm{AP}}$, using the MTJ in the DyCML circuit deteriorates the energy-delay tradeoff.

Comparison between the writing energy of the MTJ and the energy-per-operation result from our simulations indicates that the MTJ-based logic circuit requiring MTJ switching is hardly power efficient. An MTJ-based field-programmable gate array, in which MTJs only need to be written once for any logic function, may be a more suitable application for MTJ devices than standard logic. This is the focus of our ongoing research.

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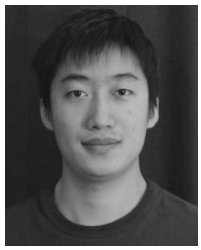

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