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An 8-Bit Compressive Sensing ADC With 4GS/s Equivalent Speed Utilizing Self-Timed Pipeline SAR-Binary-Search

Boyu Hu, Fengbo Ren, Zuow-Zun Chen, Xicheng Jiang *Fellow, IEEE,* and Mau-Chung Frank Chang, *Fellow, IEEE*

***Abstract*— This brief presents a 65nm CMOS single-channel 8-bit ADC compatible for energy-efficient high-speed Compressive Sensing (CS) and Nyquist Sampling (NS). A self-timed pipeline two-stage SAR-Binary-Search (BS) architecture is proposed and integrated with a 4GHz random-matrix clock generator, enabling a physical sampling speed up to 500MS/s with 40.2dB SNDR in NS-mode, and an equivalent speed up to 4GS/s with 36.2dB SNDR in CS-mode, leading to a FOM of 239fJ/conversion-step and 71fJ/conversion-step respectively. A Passive-charge-sharing (PCS) with open-loop (OL) residue-amplifier (RA) technique is proposed to boost the maximum physical sampling speed and the equivalent CS acquisition bandwidth. A reference-voltage fitting calibration scheme is applied to pre-distort inter-stage errors.**

***Index Terms*— Compressive Sensing, ADC, SAR-Binary-Search, Self-Timed-Pipeline**

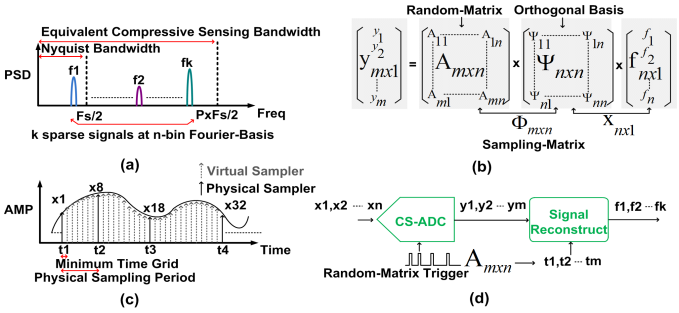

Fig. 1. (a) Spectral sparse signal; (b) Math equation describing compressive-sensing procedure; (c) Random-sampling in time-domain; (d) Mapping from math equation to hardware

I. Introduction

CONVENTIONAL signal acquisition follows Nyquist-Sampling (NS) theorem: the sampling rate should be at least twice the maximum frequency presented in a signal. Actually, many of the natural signals have more compact, or so called "sparser" representations, on a certain basis, which means a small portion of coefficients in the sparse domain are sufficient to carry a significant portion of the signal energy. Compressive Sensing (CS) theory [1] takes advantage of such fact and suggests an alternative data acquisition framework that can indirectly access the signal information in its sparse domain at sub-Nyquist rate.

Spectral sparse signals, which have sparse coefficients representation on Fourier-basis, are widely encountered in signal processing. Concrete examples include sparse spectrum sensing in Cognitive-Radio [2], transmitter localization in intelligent communication, narrow-band modulated signals with unknown carrier frequency located in wide-band, slowly-varying chirps, smooth/piecewise smooth signals and so on [3]. By incorporating randomness into the sampling process in CS-framework, spectral sparse signal information can be well encoded into much fewer samplers than that of Nyquist-Sampling, and the original signal can be robustly recovered in digital domain by applying sparsity as prior knowledge given the random-matrix. In addition, recent research [2,4] show promising and powerful signal processing techniques to solve such problems as detection, classification and filtering directly on the compressed data domain with low-complexity computations instead of resorting to a computation-consuming full-scale signal recovery. Such a trend makes the CS-framework a potentially power- and hardware-efficient alternative solution to its NS-framework counterpart for sparse signal processing.

Inspired by the encouraging progress from the signal processing community, hardware implementation of CS-based signal acquisition system has recently attracted attention from the circuit design community [5-8]. However, there still lacks combining the power of CS with high-speed CMOS ADC, which is essential in the CS signal processing toolkit.

This brief presents a CMOS ADC silicon-prototype for energy-efficient multi-GHz range spectral sparse CS operation. A self-timed pipeline scheme is proposed to combine the randomness embedded sampling and conversion with high-speed pipeline architecture. A passive-charge-sharing (PCS) technique together with open-loop residue amplifier (RA) is exploited for high-speed power-efficient inter-stage residue transferring. A two-stage architecture hybriding a SAR-ADC and Binary-Search (BS) ADC is proposed to both shorten the pipeline cycle and absorb inter-stage gain-error and non-linearity with corresponding calibration techniques. These, together with the integration of an on-chip single pulse random-matrix clock generator, lead to a 8-bit 500MS/s ADC in Nyquist-mode and equivalent 4GS/s ADC in CS-mode.

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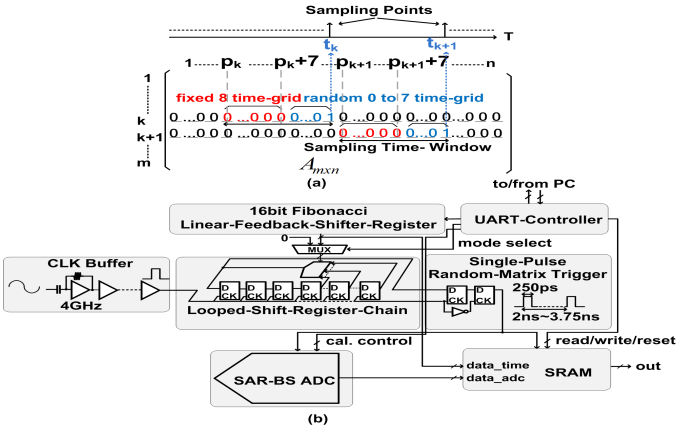

Fig. 2. (a) Random-matrix; (b) System diagram at chip-level

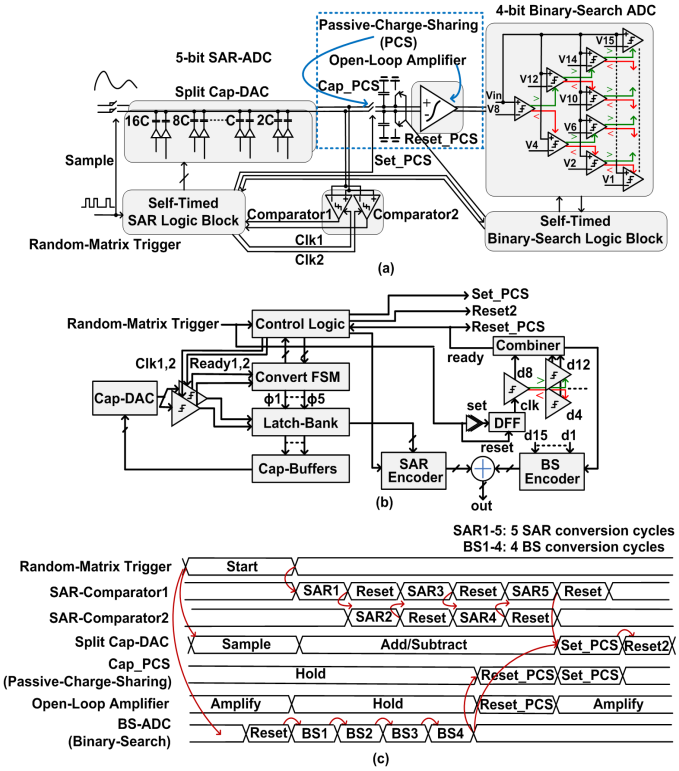

Fig. 3. (a) Proposed self-timed pipeline SAR-BS ADC architecture; (b) Proposed self-timed pipeline scheme; (c) Timing-diagram

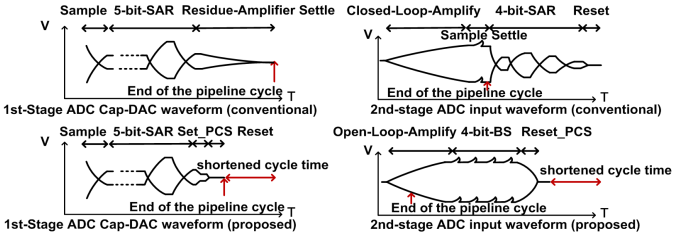

Fig. 4. Waveform of 1st-stage ADC Cap-DAC and 2nd-stage ADC input in conventional and proposed architecture

II. ADC ARCHITECTURE AND IMPLEMENTATION

A. Hardware Mapping of CS-ADC System

A conceptual explanation and its math description for the acquisition of spectral sparse signals with CS-ADC is shown in Fig.1(a) and (b). For a sparse spectrum on n-bin discrete-Fourier-basis, represented by a vector $f_{n\times1}$, only k bins (k≪n) $f_1 \cdots f_k$ contains significant coefficients. According to CS theory, m random measurements from the signal, where m satisfies [5]

$$m > k \times log_2(n) \tag{1}$$

would be sufficient to recover the original k coefficients if the sampling process adopts a known random-matrix $A_{m\times n}$. The time-domain representation of $f_{n\times1}$ is

$$x_{n\times1} = \Psi_{n\times n} \times f_{n\times1} \tag{2}$$

where $\Psi_{n\times n}$ is an orthogonal basis projection from frequency-domain to time-domain. Combining $A_{m\times n}$ and $\Psi_{n\times n}$ leads to the sampling-matrix in frequency-domain as:

$$\Phi_{m\times n} = A_{m\times n} \times \Psi_{n\times n} \tag{3}$$

(3) encodes $f_1 \cdots f_k$ into the compressed measurement as $y_{m\times1}$ in CS-operation instead of $x_{n\times1}$ in conventional NS-operation.

Fig.1(c) and (d) shows the sampling procedure in time-domain and its hardware mapping. The procedure can be considered as first sampling the input signal uniformly with "virtual" samplers at time intervals of a minimum time grid Δt_{min}, and then picking up the physical samplers from them following the random-matrix $A_{m\times n}$. Δt_{min} corresponds to the pre-defined physical time intervals between any two neighboring elements in a same row of $A_{m\times n}$. The equivalent CS acquisition bandwidth is given by the inverse of Δt_{min} while the compression-rate, which relates to the tolerable input signal sparsity levels, is defined by the average physical sampling period over Δt_{min}. As shown in Fig.2(a), each row of $A_{m\times n}$ is designed to contain only one sampling time-window. For row k, its time-window is composed of a fixed part of $8\Delta t_{min}$ from p_k to p_k+7 and a subsequent variable part randomly being $q\Delta t_{min}$ where q uniformly distributed among 0 to 7. "1" indicates a physical sampling initiated by a single-pulse-trigger while "0" indicates no physical action. The starting point p_{k+1} of the next row k+1 begins right after row k's sampling point. Since there is no overlapping between any of the sampling time-windows, the two-dimension $A_{m\times n}$ can be flattened onto the one-dimension time axis. A math expression for the consecutive sampling time points is:

$$t_{k+1} = t_k + (8+q) \times \Delta t_{min} \tag{4}$$

Fig.2(b) shows the system diagram at chip level. The ADC is integrated with a UART-controller, a SRAM and a random-matrix clock generator. The circuit implementation of the random-matrix clock generator providing the single-pulse trigger includes a TSPC-logic-based length variable looped shift register chain controlled by a digital synthesized 16-bit Fibonacci linear-feedback-shifter-register (LFSR) [6]. Δt_{min} is set as 250ps, and thus the average physical sampling time period for collecting one measurement is between 2ns to 3.75ns, leading to a 4GS/s equivalent CS-ADC with maximum physical sampling speed of 500MS/s. The NS-operation is enabled by providing the ADC with fixed time period trigger of $8\Delta t_{min}$. The SRAM is controlled by the UART-controller

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and serves as a high-speed buffer to cache both ADC's output and random sampling time intervals q. $A_{m\times n}$ is reconstructed with the recorded q values and the spectral sparse signal is recovered with ADC's output, $A_{m\times n}$ and DFT basis $\Psi_{n\times n}$ in a block-by-block way. A block size of a maximum n of 2048 and a correspondingly measurement number m of 178 on average is supported for one block recovery in the prototype. Signals that have sparse coefficients on Fourier-basis within the time interval of such one block can be acquired and recovered. This claim also applies to short-time spectral sparse signals with different sparse coefficient location and amplitude within different time intervals [3].

B. Self-Timed Pipeline SAR-Binary-Search Architecture

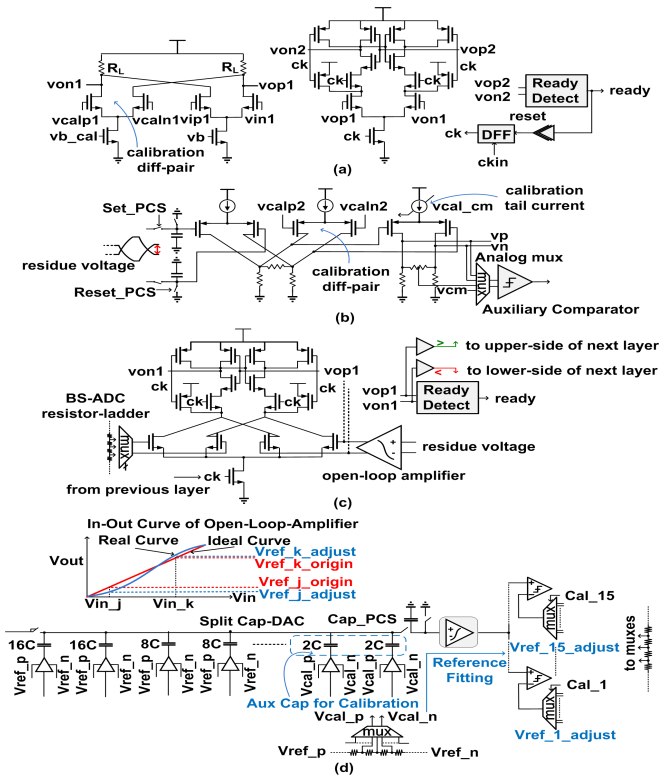

Fig. 5. (a) Comparator in SAR-ADC; (b) Passive-charge-sharing with open-loop-amplifier; (c) Comparator in BS-ADC; (d) Reference-voltage-fitting calibration

Higher maximum physical sampling speed enables wider equivalent CS acquisition bandwidth for a given compression-rate. Energy-efficient high-speed ADC architecture being able to follow random-matrix sampling is essential for wide-band CS acquisition. The proposed ADC evolves from two-stage pipeline SAR-ADC. While inheriting its good balancing between power and speed, several new techniques at both architecture and circuit level are exploited to fulfill the request of high-speed CS operation.

Fig.3(a) shows the proposed ADC architecture, which hybrids a 5-bit comparator-interleaved SAR-ADC [9] with a 4-bit BS-ADC with 1-bit overlap for over-range correction. Instead of conventional closed-loop based inter-stage residue amplification, a passive-charge-sharing scheme together with open-loop amplifier is exploited here.

Fig.3(b) shows the proposed self-timed pipeline scheme. Unlike conventional multi-phase driven pipeline scheme, the proposed pipeline operation is self-propagated. The initiation of one operation is pulse-triggered by the completion of its previous event, which makes the proposed ADC fully compatible with randomness embedded single-pulse sample and conversion. Fig.3(c) explains the timing diagram of the proposed ADC. A single-pulse from the random-matrix clock generator initiates the pipeline cycle. For the SAR-ADC, the two comparators alternatively trigger each other with their ready signals, while their compare decisions are latched to flip the split Cap-DAC, which has a unit capacitor size of 2fF. After 5-cycles, the control logic holds the operation of the SAR-ADC. For the BS-ADC, a delayed version of the random-matrix clock generator's pulse first resets and then sets the conversion clock of its 1st layer of the binary-search tree. The clock propagates through the 4 layers binary-search tree and its ready signal resets the PCS capacitor in front of the open-loop-amplifier and also send into the control logic. After receiving ready signal from both the SAR and BS ADC, the control logic sets up the PCS capacitor sample signal and then resets the split Cap-DAC, to set up for the next pipeline cycle.

The benefits on both speed enhancement and calibration feasibility brought by the proposed architecture and techniques over conventional two-stage SAR-ADC is demonstrated in Fig.4. In the conventional approach, the Cap-DAC of the 1st-stage ADC is unavailable for the next pipeline cycle until the residue amplifier is fully settled.The settling time occupies the conversion period of both two-stages and severely delays the total pipeline cycle. In the proposed approach, the Cap-DAC shares its residue passively with the PCS capacitor and then is free for the next pipeline cycle. Since the charge-sharing time is decided by the R-C time constant of the switch and the capacitor instead of the gain-bandwidth-product of the residue amplifier in close-loop configuration, the time needed for inter-stage residue transferring is significantly shortened for the 1st-stage. Notice that the 2nd-stage of the proposed architecture is a BS-ADC which directly compares the output of the residue amplifier with its pre-set voltage levels on a resistor-ladder. Its conversion speed is considerably faster than that of a conventional SAR-ADC due to the elimination of sampling and adding/subtracting voltage residue on a Cap-DAC. By properly design, the total time of open-loop-amplifier settling plus 4-bit BS conversion can be comparable to 5-bit SAR conversion plus passive-charge-sharing, which makes the pipeline cycle of the proposed two-stage architecture well-balanced and much shortened than conventional approach. The inter-stage gain error and non-linearity of the residue amplifier can be absorbed into this architecture due to the feasibility of BS-ADC's inherent analog predistortion with its reference resistor-ladder. Expensive high order polynomial fitting in digital domain would be required for the similar predistortion in SAR-ADC.

C. Circuit Implementation and Calibration Techniques

Fig.5(a) shows the comparator in the SAR-ADC. Each comparator is composed of an offset-calibrated pre-amplifier, a

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self-reset strong-arm latch and a ready detector. Fig.5(b) shows the passive-charge-sharing and open-loop-amplifier block. It is composed of a pair of top-plate-sample capacitors and a two-stage resistor load based amplifier, of which the input offset and output common-mode are calibrated with the help of a shared auxiliary comparator. The output of the amplifier is directly connected to the 15 comparators of the 4-bit BS-ADC. It serves the role of both amplifying the residue and protecting the residue from the kick-back noise of the BS-ADC. As shown in Fig.5(c), each of the comparators has a dual-differential-input, one pair of which connects to the input and the other connects to the adjustable reference voltages from the reference resistor-ladder. For a 4-layer binary-search tree of 1-2-4-8 comparators respectively, the decision result from one layer decides the propagation direction of the clock signal to its next layer.

The foreground calibrations are carried by the UART controller. For offset-calibration of both SAR comparators and open-loop-amplifier, the output of SAR's Cap-DAC is connected to common-mode voltage and the reference voltage to the calibration differential pair of the comparator or amplifier is swept step by step and frozen when the polarity of the comparator/auxiliary comparator's output flips. For common-mode calibration of the open-loop-amplifier, the analog mux redirects the input of auxiliary comparator to the amplifier's common-mode and the common-mode of BS-ADC's resistor ladder. The calibration tail current of its 2nd-stage is adjusted until these two voltages match. Fig.5(d) shows the applying of inter-stage reference-voltage fitting calibration scheme. For each of the 15 comparators in the BS-ADC, its reference voltage can be adjusted +2/-2 LSB around the original voltage with a step of 1/4 LSB. During calibration, a combined usage of the calibration capacitor in the Cap-DAC and a 4-bit resistor-DAC generates 15 calibration voltages from -7 LSB to 7 LSB, one corresponding to calibration of BS-ADC's each comparator. The reference voltage of each comparator is swept from low to high until its output polarity flips. Since the calibration voltages are generated on the signal path and experience the same passive-charge-sharing and open-loop-amplifying process as normal input signal, the signal path imperfectness, including the inter-stage gain-error, offset and non-linearity, and the comparator's offset of the BS-ADC, is analog pre-distorted through this calibration procedure[15].

III. EXPERIMENT RESULTS

The proposed ADC has been designed and fabricated in standard 65nm CMOS technology. The output signals are post-processed and recovered based on Orthogonal-Matching-Pursuit [10-11].

Fig.6 presents the die micrograph. Fig.7 shows the DNL and INL performance. The DNL is -0.6/+1.5 LBS and the INL is -0.8/+1.4 LBS after calibration. Fig.8 presents the SFDR and SNDR performance in NS-mode, and in CS-mode with post-processing and recovery, as the input frequency changes.

Fig. 9 plots the decimated-by-64 output spectrum for an input signal of 0.73MHz in NS-mode with SNDR of 40.2dB and SFDR of 47.7dB.

Fig.10 shows the detection of a 3% sparsity input signal composed of 30 active frequency bins randomly located across 0-2GHz frequency band. The detection accuracy is 100%.

Fig.11 shows the acquired spectral sparse two-band Amplitude-Modulated (AM) signal with carriers located at 404MHz and 1186MHz, respectively. Fig.12 shows the de-modulated 2 baseband signals from acquisition and the ideal ones generated in Matlab. Each baseband signal is represented by 6 coefficients randomly located on discrete-Fourier-basis within 30MHz. The time-domain recovery SNDR, which is defined by the ratio of normalized ideal signal amplitude over the normalized maximum deviation of recovered signal from ideal signal, are 37dB and 36dB, respectively, including all the errors from arbitrary-waveform-generator, cables, connectors and PCB.

TABLE I summarizes the performance of the prototype and its comparison with state-of-art NS and CS ADCs. A 40x wider acquisition bandwidth is achieved compared with its prior art CS counterpart. It also shows significant power and area reduction compared with its NS-ADC counterparts by exploring CS for wideband located spectral sparse signals.

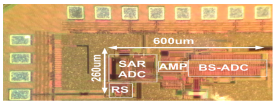

Fig. 6. Die micrograph of the ADC

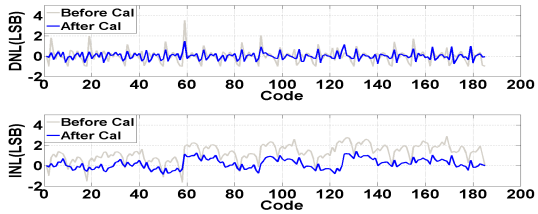

Fig. 7. Measured DNL and INL performance before and after calibration

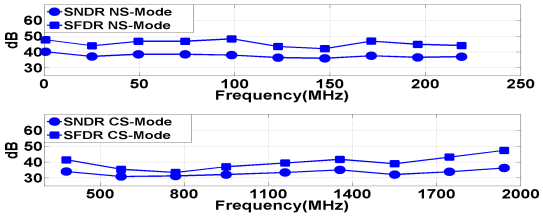

Fig. 8. Measured SNDR and SFDR performance as the input frequency changes in NS-mode and CS-Mode (with post-processing and recovery)

IV. CONCLUSION

A single-channel 8-bit CS/NS ADC silicon prototype integrated with a high-speed random-matrix clock generator is presented. With the proposed self-timed pipeline SAR-BS architecture, the ADC achieves a physical sampling speed up

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TABLE I
SUMMARY OF PERFORMANCE COMPARISON

	This Work		[5] TCAS-I 13		[12] CICC 13	[13] JSSC 13	[14] ASSC 13
Architecture	Single-Channel(SC)		SC		4-way TI	SC	2-way TI
Sampling-Mode	Nyquist	CS	Nyquist	CS	Nyquist	Nyquist	Nyquist
Resolution(bit)	8		10		8	6	4
SNDR(dB)Low/Nyquist	40.2/37.1	-/36.2	57.6/49.9	-/55.9	-/44.4	-/31.2	-/24.1
Fs(MHz)	500	4000*	9.5	100*	4000	4100	4000
Power(mW)	10**	15***	0.55**	0.63***	120	76	20
FOM(fJ/CS)	239	71	92	12	219	625	378
DNL(LSB)	-0.6/+1.5		-1/+0.5		-0.75	+0.49/-0.48	+0.18/-0.18
INL(LSB)	-0.8/+1.4		-1/+1		-1.5	+0.74/-0.74	+0.11/-0.11
Technology(nm)	65		90		65	90	65
Active-Area(mm^2)	0.16		0.15		1.35	0.38	0.15
*Equivalent sampling speed **Core consumption ***With random-matrix generator							

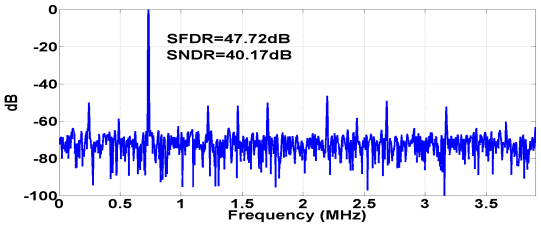

Fig. 9. Measured output spectrum for an input signal of 0.73MHz in NS-mode with a decimation of 64

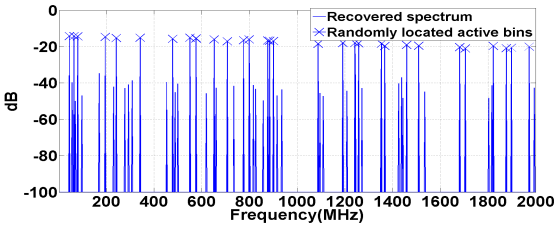

Fig. 10. Measured output spectrum of a 3% spectral sparse signal

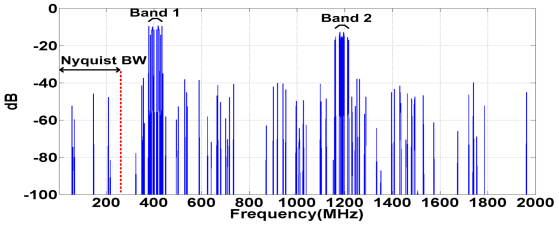

Fig. 11. Measured output spectrum of a spectral sparse two-band AM signal

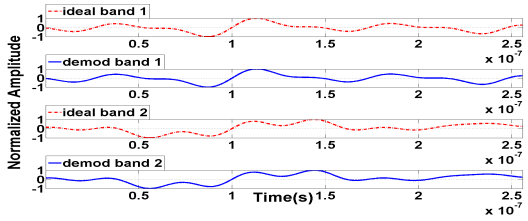

Fig. 12. Ideal and demodulated two baseband signals

to 500MS/s, and an equivalent speed up to 4GS/s for spectral sparse signal processing applications. A passive-charge-sharing with open-loop-amplifier technique is proposed to effectively shorten the pipeline cycle and improves the conversion energy-efficiency. The applying of inter-stage reference-voltage fitting calibration scheme into the proposed architecture is also investigated.

REFERENCES

[1] Candes, Emmanuel J., Justin Romberg, and Terence Tao. "Robust uncertainty principles: Exact signal reconstruction from highly incomplete frequency information." *IEEE Trans. Inf. Theory*, vol.52, no.2, pp. 489-509, Feb. 2006.

[2] Tian, Zhi, and Georgios B. Giannakis. "Compressed sensing for wideband cognitive radios." *2007 IEEE International Conference on Acoustics, Speech and Signal Processing, (ICASSP)*, vol.4, pp. 1357-1360, April.2007.

[3] Tropp, Joel, et al."Beyond Nyquist: Efficient sampling of sparse bandlimited signals" *IEEE Trans. Inf. Theory*, vol.56, no.1, pp. 520-544, Jan. 2010.

[4] Davenport, Mark, et al. "Signal processing with compressive measurements" *IEEE J. Emerging and Selected Topics in Signal Processing.*, vol.4, no.2, pp. 445-460, April. 2010.

[5] M. Trakimas, et al. ,"A compressed sensing analog-to-information converter with edge-triggered SAR ADC core." *IEEE Trans. Circuits Sys. I, Reg. Papers* , vol.60, no.5, pp.1135-1148, May. 2013.

[6] Bellasi, David E., et al.,"VLSI design of a monolithic compressive-sensing wideband analog-to-information converter." *IEEE J. Emerging and Selected Topics in Circuits and System.*, vol. 3, no.4, pp. 552-565, Apr. 2013.

[7] Chen, Xi, et al ,"A sub-Nyquist rate sampling receiver exploiting compressive sensing" *IEEE Trans. Circuits Sys. I, Reg. Papers* , vol.58, no.3, pp.507-520, Mar. 2011.

[8] Chen, F., et al ,"Design and Analysis of a Hardware-Efficient Compressed Sensing Architecture for Data Compression in Wireless Sensors" *IEEE J. Solid-State Circuits*, vol.47, no.3, pp.744-756, Mar. 2012.

[9] Kull, Lukas, et al. ,"A 3.1 mW 8b 1.2 GS/s single-channel asynchronous SAR ADC with alternate comparators for enhanced speed in 32 nm digital SOI CMOS." *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 3049-3058, Dec. 2013.

[10] Tropp, Joel A., and Anna C. Gilbert. , "Signal recovery from random measurements via orthogonal matching pursuit." *IEEE Trans. Inf. Theory*, vol. 53, no.12, pp. 4655-4666, Dec. 2007.

[11] Ren, Fengbo, et al. , "A configurable 12-to-237KS/s 12.8mW sparse-approximation engine for mobile ExG data aggregation." *2015 IEEE Int. Solid-State Circuits Conf (ISSCC) Dig. Tech. Papers*, pp.1-3.

[12] Wei, Hegong, et al. , "An 8-Bit 4-GS/s 120-mW CMOS ADC." *IEEE Custom Integrated Circuits Conference*, pp.1-4, Sept. 2013

[13] Kim, Jong-In, et al. " A 6-b 4.1-GS/s flash ADC with time-domain latch interpolation in 90nm CMOS." *IEEE J. Solid-State Circuits*,vol. 48, no. 6, pp. 1429-1441, June. 2013.

[14] Yousry Ramy, et al., " An architecture-reconfigurable 3b-to-7b 4GS/s-to-1.5GS/s ADC using subtractor interleaving." *2013 IEEE Asian. Solid-State Circuits Conf*, pp. 285-288, Nov. 2013.

[15] Hashemi, S., et al., " A 7.1-mW 1-GS/s ADC with 48-dB SNDR at Nyquist Rate." *IEEE Custom Integrated Circuits Conference*, pp.1-4, Sept. 2013.