9-bit time–digital-converter-assisted compressive-sensing analogue–digital-converter with 4 GS/s equivalent speed

B. Hu✉, F. Ren, Z.-Z. Chen, X. Jiang and M.-C.F. Chang

A novel 9-bit time–digital-converter (TDC)-assisted analogue–digital-converter (ADC) supporting energy-efficient high-speed compressive-sensing (CS) operation is presented. With a voltage–time-converter serving as the cross-domain residue conveyer, the proposed two-stage self-timed pipeline ADC architecture hybrids a voltage-domain comparator-interleaved successive-approximation (SAR) ADC front-end and a time-domain locally readjusted folding two-dimensional Vernier TDC back-end. Implemented in 65 nm CMOS technology, the prototype benefits from both the CS-enabled sub-Nyquist operation and the hybrid quantisation scheme, leading up to 4 GS/s equivalent speed with 34.2 dB signal-noise-distortion-ratio (SNDR) and a figure-of-merit (FOM) of 101 fJ/conversion step.

Introduction: Signal sparsity is defined as the ratio of the amount of signal coefficients containing effective information over that of the total amount on certain transform basis. Many of the emerging applications involve sparse signal processing; such as spectrum sensing in cognitive-radio (CR) [1]. For a sparse frequency spectrum consisting of n bins, only k bins ($k \ll n$) f_1, …, f_k are active at a given moment and need detection. Directly capturing this sparse spectrum with the Nyquist-sampling (NS) analogue–digital-converter (ADC) at a speed twice the maximum frequency component f_k would be extremely power hungry and hardware inefficient. An alternative and more elegant solution is to utilise the recently developed compressive-sensing (CS) theory [2], which indicates that a substantially lower measurement of m with a lower bound of $k \times \log2(n)$ would be sufficient to recover the original k coefficients if the sampling procedure follows known non-uniform sampling time points t_1, …, t_m, as shown in Fig. 1*a*. The sample interval between any two consecutive sampling points t_k and t_{k+1} is a minimum time grid multiplied by a random integer. The equivalent CS acquisition bandwidth is the inverse of this minimum time grid. Pulse triggered at the non-uniform sampling time points, the CS-ADC captures the signal with a sub-Nyquist average physical sampling period, the ratio of which over the minimum time grid defines the compression rate. The captured signal y_1, y_2, …, y_m is then recovered in frequency domain with the provided prior information of sample intervals.

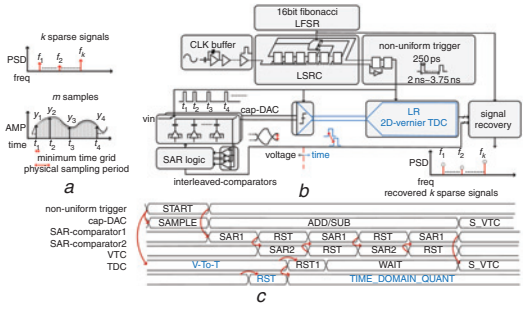

Fig. 1 *Proposed TDC-assisted CS-ADC*

a Randomness embedded non-uniform sampling concept
b ADC system architecture
c Timing diagram

Although research on CS theory is blooming, the hardware implementation of such concept is limited [3–4].

This Letter presents a novel digital-intensive 9-bit time–digital-converter (TDC)-assisted ADC supporting CS as well as NS operation. As shown in Fig. 1*b*, the two-stage self-timed pipeline architecture hybrids a voltage-domain 5-bit comparator-interleaved SAR-ADC and a time-domain 5-bit locally readjusted folding two-dimensional (2D)-Vernier TDC with 1-bit redundancy. The voltage-domain RA is replaced by a cross-domain voltage–time-converter (VTC). The proposed hybrid voltage–time-domain solution provides the following advantages. First, the operation of VTC and TDC are fully self-timed, thus can be energy-efficiently initiated by the non-uniform sampling pulse triggers. Second, the long settling time of RA is eliminated from the pipeline cycle by using the VTC, significantly improving the speed. Third, both the VTC and TDC are composed of digital-intensive logic circuits, improving the energy efficiency under non-uniform operation.

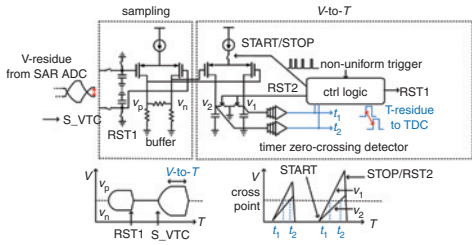

Fig. 2 *Proposed VTC*

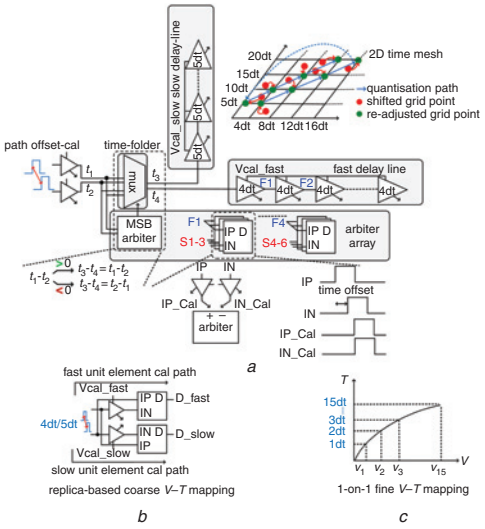

Fig. 3 *Proposed locally readjusted folding 2D-Vernier TDC*

a Circuit implementation
b Coarse calibration
c Fine calibration

Circuit implementation: Randomness embedded sampling is achieved by clocking the ADC core with a single-pulse non-uniform trigger in CS operation. As shown in Fig. 1*b*, to ensure that the minimum physical sampling time period is no shorter than the ADC conversion period, each time period is composed of a fixed part and a variable part. A true-single-phase-clock (TSPC) logic-based length variable looped shift register chain provides a combination of fixed eight minimum time grids and variable 0–7 minimum time grids, 250 ps of each, while the variable part is controlled by a digital synthesised 16-bit Fibonacci linear-feedback-shifter-register for randomness generation [4]. In CS mode, the ADC samples the sparse frequency-domain input signal with a variable time period from 2 to 3.75 ns, providing 4 GS/s equivalent speed. By providing a fixed time period of 2 ns, the ADC can work as a general-purpose NS-ADC with a speed of 500 MS/s.

Fig. 1*c* shows the timing diagram of the proposed hybrid ADC architecture. Different from the conventional approach, the pipeline cycle is fully self-propagated, capable of being initiated by the single-pulse non-uniform trigger. On the front-end, after sampling the input signal with the cap-DAC, the two interleaved comparators [5] of the SAR ADC solve the 5-bit most-significant-bit (MSB) by alternatively triggering each other with their conversion ready signals, and the decision result flips the cap-DAC. After finishing the SAR conversion, a sample signal given by the self-timed SAR-logic shares the residue charge on SAR ADC's cap-DAC with the sampling capacitor of the VTC. A following reset signal clears up the cap-DAC and ends the pipeline cycle. On the back-end, the sampled residue charge is converted into time domain by the VTC, after when the VTC's sampling capacitor is reset by its self-timed control logic. The time-domain residue then automatically triggers the quantisation procedure of the TDC.

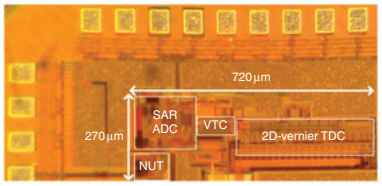

Fig. 4 *Die micrograph of ADC*

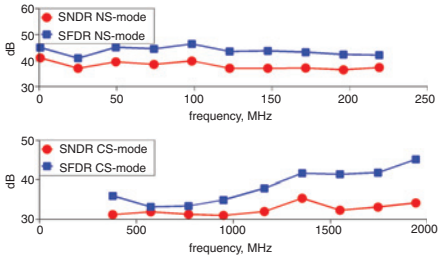

Fig. 5 *Calibrated SNDR and SFDR performance as input frequency changes in NS mode and CS mode*

Fig. 2 shows the cross-domain residue conveying procedure, which replaces the conventional voltage-domain residue amplifying. The VTC is composed of a buffer, a timer and a zero-crossing detector. The buffer protects the sampled residue charge from the kick-back noise of the timer. Triggered by the non-uniform single pulse, the timer starts to charge its loading capacitors. A crossing of the inherent voltage threshold of the inverter-based zero-crossing detector triggers its output to flip from low to high. When both of the detector's output goes high, the self-timed control logic disconnects the current source and resets the loading capacitors. In this way, the sampled voltage residue is transformed into the rising-edge time difference between the outputs of the zero-crossing detector.

A 2D-Vernier-TDC [6] pairs each element on the fast delay line with multiple elements on the slow delay line, thus significantly reducing the total number of delay elements needed and boosting the conversion speed. However, this 2D implementation unavoidably leads to non-equivalent arbiter numbers at different delay-element's output nodes. The unevenly distributed capacitance loading shifts the time grids away from their original positions on the 2D time mesh and introduces a systematic quantisation error. The issue is mitigated by modifying the architecture into a proposed locally readjusted one. As shown in Fig. 3*a*, a pair of calibration delay elements is embedded inside each of the time arbiters, providing one more degree of freedom to the time mesh. By calibration, the shifted grid points can be readjusted to their original position on the quantisation path, effectively alleviating the performance degradation. To further reduce the power consumption, a 1-bit time folder, which is a pair of multiplexers (MUXs) controlled by the MSB arbiter, converts the negative input time differences into positive ones and thus reduces the number of necessary time arbiters by half.

Various calibrations are implemented in this hybrid architecture. First, the differential time path offset from VTC to the time folder is calibrated by balancing the delay lines between them. Second, a coarse voltage–time mapping is set up by calibrating the absolute delay of replica unit element of fast line/slow line to 4dt/5dt (1t is 1least-significant-bit (LSB) of TDC), as shown in Fig. 3*b*. Third, each time arbiter is locally readjusted by a 1-on-1 fine mapping from voltage to time domain as shown in Fig. 3*c*. The procedure is self-calibration based. All of the time-domain calibration signals are generated by reconfiguring the front-end SAR cap-DAC and conveying through the VTC. In addition, the output code of SAR ADC and the TDC are adjusted in digital domain to alleviate the signal offset and asymmetry in the time-folding procedure.

Experimental results: The ADC prototype is fabricated in standard 65 nm CMOS technology. The die photo is shown in Fig. 4. The signal recovery algorithm is based on orthogonal-matching pursuit. Fig. 5 shows the calibrated spurious-free-dynamic-range (SFDR) and SNDR performance of the ADC operating in both NS mode and CS mode. It achieves 40.8 dB SNDR at low frequency in NS mode and 34.2 dB SNDR near 2 GHz in CS mode. Table 1 summarises the performance of the prototype and its comparison with state-of-art CS and NS ADCs. With the proposed hybrid architecture, it achieves 40× increase of acquisition bandwidth compared with its prior art CS-operation counterpart. It also shows significant energy-efficiency advantages over its NS-operation counterparts for sparse frequency-domain signal acquisition.

Table 1: Performance summary and comparison with prior arts

	This work	TCAS-I13 [3]	JSSC13 [7]	ASSCC13 [8]
Sample mode	CS	CS	NS	NS
Resolution	9	10	6	4
Sample rate (GS/s)	4[a]	0.1[a]	4.1	4
Power (mW)	17	0.63	76	20
SNDR (dB)	34.2	55.9	31.2	24.1
FOM (fJ/CS)	101	12	625	378
Active area (mm^2)	0.194	0.15	0.38	0.15
Architecture	SAR + TDC	SAR	flash	flash
Technology (nm)	65	90	90	65

[a]Equivalent sampling speed.

Conclusion: A single-channel 9-bit TDC-assisted CS-ADC is presented. The proposed novel hybrid voltage–time-domain architecture enables up to 4 GS/s equivalent speed with a FOM of 101 fJ/conversion step. It provides a highly digital-intensive energy-efficient high-speed ADC candidate for sparse frequency-domain signal acquisition as well as general purpose data conversion applications.

Submitted: *5 November 2015* E-first: *25 February 2016*
doi: 10.1049/el.2015.3778
One or more of the Figures in this Letter are available in colour online.

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